Four-Channel Transimpedance Amplifier with Output Multiplexing

FEATURES

- 600MHz –3dB Bandwidth with 0.5pF Input Capacitance
- Differential Output with Up to $2V_{P-P}$ Swing into 100Ω Differential Load
- Built-In High-Speed ADC Driver with Output MUX
- Selectable 22.2/16.7/11.1/5.55kΩ Transimpedance Gain
- 1.8pA/3.7pA$\sqrt{Hz}$ Input Current Noise Density 100MHz/600MHz (0.5pF)
- $65nA_{RMS}$ Integrated Input-Referred Current Noise Over 600MHz (0.5pF)
- Large Linear Input Current Range 0µA to 90µA
- Large Transient Overload Current >1A Peak
- Fast Overload Recovery: 2.5ns
- Fast Channel Switching: 10ns
- Power Dissipation: 194mW to 325mW on 3.3V, Varies with Output Mode (13mW in Shutdown)
- Output MUX allows multiple LTC6563s to Create 8, 12, 16 … 32 Channel Solutions
- 3mm × 5mm, 24-Lead QFN Package, Wettable Flanks
- AECQ-100 Grade 1 Qualified (Pending)

APPLICATIONS

- Automotive LIDAR Receiver
- Industrial LIDAR Receiver

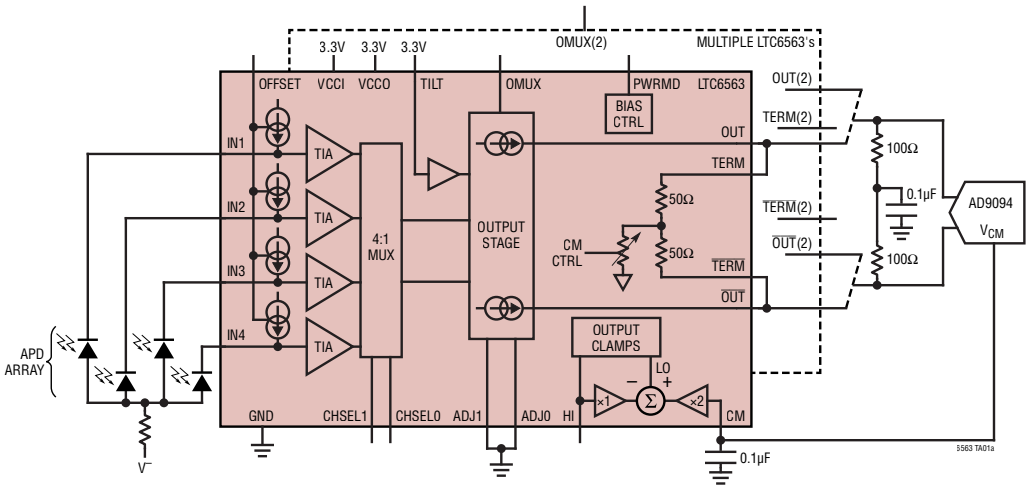
DESCRIPTION

The LTC®6563 is a low-noise four-channel transimpedance amplifier (TIA) with 600MHz bandwidth. The LTC6563 TIA's low noise, wide linear range, and low power dissipation are ideal for LIDAR receivers using Avalanche photodiodes (APDs) and photodiodes (PDs). The amplifier features selectable 22.2/16.7/11.1/5.55kΩ Transimpedance gain (RT) and 90µA linear input current range. Using an APD with a total input capacitance of 0.5pF, the input current noise density is 1.8pA/$\sqrt{Hz}$ at 100MHz and 3.7pA/$\sqrt{Hz}$ at 600MHz. The LTC6563 consumes between 194mW and 325mW on a 3.3V supply depending on output mode. An internal 4-to-1 MUX simplifies the system design. In addition, external multiplexing capability allows channel expansion up to 64 channels, saving space and power. Fast overload recovery and fast channel switchover make the LTC6563 well suited for LIDAR receivers with multiple APDs. The built-in high-speed differential ADC driver can swing as much as $2V_{P-P}$ while driving into 100Ω external differential load.

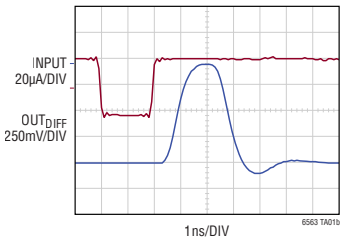
The LTC6563 is packaged in a 3mm × 5mm 24-pin exposed pad QFN package with wettable flanks.

TYPICAL APPLICATION

Typical Application with DC-Coupled Inputs Driving an ADC



Pulse Response



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage:
- V_{CCI} to GND 3.6V
- V_{CCO} to GND 3.6V

Input Current (CHSEL0, CHSEL1, ADJ0, ADJ1, PWRMD, OMUX, CM, HI, OFFSET, TILT) ..... ±10mA

Amplifier Inputs (IN1, IN2, IN3, IN4):
- Voltage..... –0.3V to 3.6V
- Current..... 10µA/–400mA$_{RMS}$
- Current (Note 5)..... –1A Transient

Amplifier Outputs (OUT, $\overline{OUT}$):
- Voltage..... –0.3V to 3.6V
- Current..... ±100mA

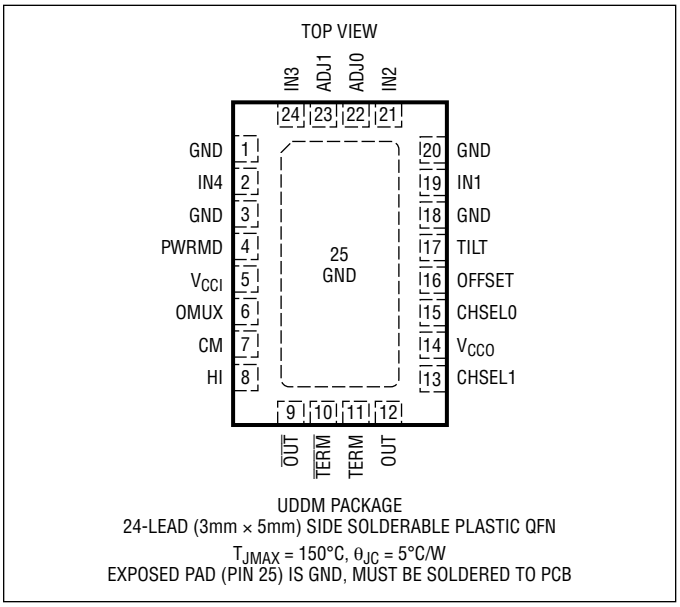
Amplifier Output Termination (TERM, $\overline{TERM}$):
- Voltage..... –0.3V to 3.6V
- Current..... –72mA/6mA

Operating Temperature Range:
- LTC6563I (Note 2) ..... –40°C to 85°C
- LTC6563H (Note 3)..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

Junction Temperature ..... 150°C

PIN CONFIGURATION



UDDM PACKAGE
24-LEAD (3mm × 5mm) SIDE SOLDERABLE PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6563IUDDM#PBF	LTC6563IUDDM#TRPBF	LHMH	24-Lead (3mm × 5mm) Side Solderable Plastic QFN	–40°C to 85°C
LTC6563HUDDM#PBF	LTC6563HUDDM#TRPBF	LHMH	24-Lead (3mm × 5mm) Side Solderable Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, ADJ0 = ADJ1 = PWRMD = OMUX = V_{CCI} = HI = V_{CCO} = 3.3V, TILT = OFFSET = 0, V_{CM} = 1.5V. All other input pins are floating unless stated otherwise. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_{L_EXT} = 100Ω differential, OUT connected to TERM and $\overline{OUT}$ connected to $\overline{TERM}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BW	–3dB Bandwidth	200mV$_{P-P,OUT}$ and $C_{IN,TOT}$ = 0.5pF		600		MHz
SR	Slew Rate	$C_{IN,TOT}$ = 0.5pF		3000		V/us
t_R/t_F	Rise/Fall Time	$C_{IN,TOT}$ = 0.5pF		0.6		ns
R_T Differential	Small Signal Transimpedance	I_{IN} < 2μA$_{P-P}$, ADJ00 I_{IN} < 2μA$_{P-P}$, ADJ01 I_{IN} < 2μA$_{P-P}$, ADJ10 I_{IN} < 2μA$_{P-P}$, ADJ11	4.9 9.6 14.1 18.1	5.55 11.1 16.7 22.2	6.5 12.5 18.2 23.4	kΩ kΩ kΩ kΩ
TCR_T	Transimpedance Temperature Coefficient	I_{IN} < 2μA$_{P-P}$, ADJ00 I_{IN} < 2μA$_{P-P}$, ADJ01 I_{IN} < 2μA$_{P-P}$, ADJ10 I_{IN} < 2μA$_{P-P}$, ADJ11		–0.00125 –0.00246 –0.00403 –0.00609		kΩ/°C kΩ/°C kΩ/°C kΩ/°C
R_{IN}	Input Impedance	f = 100kHz Active Channel f = 100kHz Inactive Channel		225 409		Ω Ω
R_{TERM_DIFF}	Internal Diff Termination Impedance	Measured from TERM to TERMBAR		100		Ω
I_n	Input Current Noise Density	f = 100MHz, C_{IN_TOT} = 0.5pF f = 200MHz, C_{IN_TOT} = 0.5pF f = 300MHz, C_{IN_TOT} = 0.5pF f = 400MHz, C_{IN_TOT} = 0.5pF f = 500MHz, C_{IN_TOT} = 0.5pF f = 600MHz, C_{IN_TOT} = 0.5pF		1.8 2.3 2.5 3 3.4 3.7		pA/√Hz pA/√Hz pA/√Hz pA/√Hz pA/√Hz pA/√Hz
	Integrated Input Current Noise	f = 0.1MHz to 100MHz, C_{IN_TOT} = 0.5pF f = 0.1MHz to 200MHz, C_{IN_TOT} = 0.5pF f = 0.1MHz to 300MHz, C_{IN_TOT} = 0.5pF f = 0.1MHz to 400MHz, C_{IN_TOT} = 0.5pF f = 0.1MHz to 500MHz, C_{IN_TOT} = 0.5pF f = 0.1MHz to 600MHz, C_{IN_TOT} = 0.5pF		19 27 36 45 55 65		nA_{RMS} nA_{RMS} nA_{RMS} nA_{RMS} nA_{RMS} nA_{RMS}
$t_{RECOVER}$	Overload Recovery and Pulse Extension	I_{IN} = –4mA, C_{IN_TOT} = 0.5pF		2.5		ns
t_{CH_SWITCH}	Channel Switching Time	Any Channel to Any Channel		10		ns
t_{OMUX_SWITCH}	Output MUX Switching Time	OMUX		20		ns
Isolation	Channel to Channel Isolation	400MHz, PWRMD = Logic Low, Selected Channel to Any Unselected Channel		48		dB

DC ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN1, IN2, IN3, IN4 Pins							
V_{IN}	Input Bias Voltage	Active Channel Inactive Channel			0.8 0.7		V V
I_{IN}	DC Input Current Range	Tilt = 0V Tilt = 3.3V			40 90		μA μA
OUT and OUT Pins							
$V_{OCM\_DEFAULT}$	Default Output Common-Mode Voltage	ADJ = 00			0.9		V
V_{OOD}	Differential Output Offset Voltage	I_{IN} = 0μA		–75	±10	75	mV
TCV_{OOD}	Differential Output Offset Voltage Temperature Coefficient	I_{IN} = 0μA,			–0.044		mV/°C

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, ADJ0 = ADJ1 = PWRMD = OMUX = V_{CCI} = HI = V_{CCO} = 3.3V, TILT = OFFSET = 0, V_{CM} = 1.5V. All other input pins are floating unless stated otherwise. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_{L_EXT} = 100Ω differential, OUT connected to TERM and $\overline{OUT}$ connected to $\overline{TERM}$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{SWINGDIFF}$	Differential Output Voltage Swing	I_{IN} = 0 to –200µA, Tilt = 3.3V	●	1.13 1.03	1.50		V_{P-P} V_{P-P}
		I_{IN} = 0 to –90µA, Tilt = 3.3V, R_{L_EXT} = 75Ω SE on Each Output with Center Grounded (see Figure 3)			2.4		V_{P-P}
V_{OUTLOW}	Output Voltage Swing Low	Single-Ended Measurement, I_{IN} = 0 to –200µA, Tilt = 3.3V			1.02		V
$V_{OUTHIGH}$	Output Voltage Swing High	Single-Ended Measurement, I_{IN} = 0 to –200µA, Tilt = 3.3V			2.2		V
$V_{COMPLIANCE}$	Output Voltage Compliance	Single-Ended Measurement, I_{IN} = 0 to –200µA, Tilt = 3.3V		2.0	V_{CCO} –1		V
Output Common Mode Voltage Control ($_{CM}$ Pin)							
A_{CM}	CM Pin Voltage Gain, CM Pin to Differential OUT	V_{CM} = 1.5V to 1.7V		0.95	1	1.05	V/V
$TCAV_{CM}$	A_{CM} Temperature Coefficient				9.3		(µV/V)/°C
$V_{CM\_DEFAULT}$	Default CM Pin Voltage				0.9		V
V_{CM_OS}	Common Mode Offset Voltage	$V_{OUTCM} – V_{CM}$		–50	10	20	mV
TCV_{CM_OS}	Common Mode Offset Voltage Temperature Coefficient	$V_{OUTCM} – V_{CM}$			–0.021		mV/°C
V_{OUTCM_MIN}	V_{OUTCM} Minimum Voltage	V_{CM} = 0V, ADJ00			0.38	0.43	V
V_{OUTCM_MAX}	V_{OUTCM} Maximum Voltage	V_{CM} = 2.6V, ADJ11		2.2	2.3		V
R_{CM}	CM Pin Input Resistance				16.3		kΩ
C_{CM}	CM Pin Input Capacitance				1.5		pF
Output Clamping (HI Pin) See Note 4							
$V_{HI\_DEFAULT}$	Default HI Pin Voltage				1.8		V
V_{HI_VOS}	High Side Clamp Offset Voltage	$V_{OUT(MAX)} – V_{HI}$, HI = 1.7V, I_{IN} = –200µA		–160	–65	25	mV
V_{LO_VOS}	Low Side Clamp Offset Voltage	$V_{OUTBAR(MIN)} –(2 • V_{CM} – V_{HI})$, HI = 1.7V, I_{IN} = –200µA		–50	50	150	mV
R_{HI}	HI Pin Input Impedance				13.6		kΩ
C_{HI}	HI Pin Input Capacitance				1.5		pF
Input Current Cancellation (OFFSET Pin)							
$V_{OFFSET\_DEFAULT}$	Default OFFSET Pin Voltage				0		V
I_{CANCEL_MIN}	Minimum Input Cancellation Current	V_{OFFSET} = 0V			0		µA
I_{CANCEL_MAX}	Maximum Input Cancellation Current	V_{OFFSET} = 3.3V, Tilt = 3.3V		200	240		µA
G_{OFFSET}	OFFSET Pin Transconductance (OFFSET Pin Voltage to Input Offset Current)	V_{OFFSET} = 0.2V to 0.4V, I_{IN} = –40µA		–145	–110	–75	µA/V
R_{OFFSET}	OFFSET Pin Impedance				6.6		kΩ
t_{S_OFFSET}	Offset Voltage to Output Settling	1% of Final Value, I_{IN} = –40µA			100		ns
Output Offset (TILT Pin)							
$V_{TILT\_DEFAULT}$	Default Tilt Pin Voltage				2		mV
A_{TILT}	TILT Pin Slope, TILT to Differential Out	V_{TILT} = 0.2V to 0.4V		–1.25	–1	–0.7	V/V
TCA_{TILT}	A_{TILT} Temperature Coefficient	V_{TILT} = 0.2V to 0.4V			–680		(µV/V)/°C
R_{TILT}	TILT Pin Input Impedance				22.7		kΩ

DC ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADJ0, ADJ1, CHSEL0, CHSEL1 Pins with Internal Pull-Down Resistors							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.4			V
I_{IL}	Input Low Current	Pin Voltage = 0.8V			3.8		µA
I_{IH}	Input High Current	Pin Voltage = 2.4V			7.2		µA
C_{IN}	Pin Input Capacitance				1.5		pF
R_{IN}	Pin Input Impedance	To GND			218		kΩ
OMUX, PWRMD, Pins with Internal Pull-Up Resistors							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.4			V
I_{IL}	Input Low Current	Pin Voltage = 0.8V			–12		µA
I_{IH}	Input High Current	Pin Voltage = 2.4V			–8.6		µA
C_{IN}	Pin Input Capacitance				1.5		pF
R_{IN}	Pin Input Impedance	To V_{CCI}			208		kΩ
Power Supply							
V_S	Operating Supply Range			3.15	3.3	3.45	V
I_{VCCI}	Input Supply Current	Any Adjust Setting	 ●	27.8	34	39.4 40.4	mA mA
$I_{VCCI\_SHUTDOWN}$	Input Supply Current	PWRMD = OMUX = Logic Low	 ●		4.5	5.5 6	mA mA
I_{VCCO}	Output Supply Current	ADJ1 = Logic High, ADJ0 = Logic High V_{CM} = 1.50V	 ●	49.4	64.5	81 82	mA mA
		ADJ1 = Logic High, ADJ0 = Logic Low V_{CM} = 1.25V	 ●		51.5	64.9 65.9	mA mA
		ADJ1 = Logic Low, ADJ0 = Logic High V_{CM} = 1.0V	 ●		38	48 49	mA mA
		ADJ1 = Logic Low, ADJ0 = Logic Low V_{CM} = 0.75V	 ●		24.5	30.8 31.8	mA mA
$I_{VCCO\_SHUTDOWN}$	Output Supply Current	PWRMD = OMUX = Logic Low	 ●		0.1	0.2 0.22	mA mA
I_S	Total Supply Current ($I_{S(VCCI)}$ + $I_{S(VCCO)}$)	ADJ1 = Logic High, ADJ0 = Logic High V_{CM} = 1.50V	 ●		98.5	120.4 122.4	mA mA
		ADJ1 = Logic High, ADJ0 = Logic High V_{CM} = 1.25V	 ●		85.5	104.3 106.3	mA mA
		ADJ1 = Logic Low, ADJ0 = Logic High V_{CM} = 1.0V	 ●		72	87.4 89.4	mA mA
		ADJ1 = Logic Low, ADJ0 = Logic Low V_{CM} = 0.75V	 ●		58.5	70.2 72.2	mA mA
$I_{S\_SHUTDOWN}$	Total Supply Current ($I_{S(VCCI)}$ + $I_{S(VCCO)}$)	PWRMD = OMUX = Logic Low	 ●		4.6	5.8 6.3	mA mA
PSRR(V_{CCI})	Input Power Supply Rejection Ratio ($\Delta V_{OUT}/\Delta V_{CCI}$)	V_{CCI} = 3.15V to 3.45V, V_{CCO} = 3.3V		33	36		dB
PSRR(V_{CCO})	Output Power Supply Rejection Ratio ($\Delta V_{OUT}/\Delta V_{CCO}$)	V_{CCO} = 3.15V to 3.45V, V_{CCI} = 3.3V		35	38		dB

DC ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6563I is guaranteed to meet specified performance from –40°C to 85°C.

Note 3: The LTC6563H is guaranteed to meet specified performance from –40°C to 125°C.

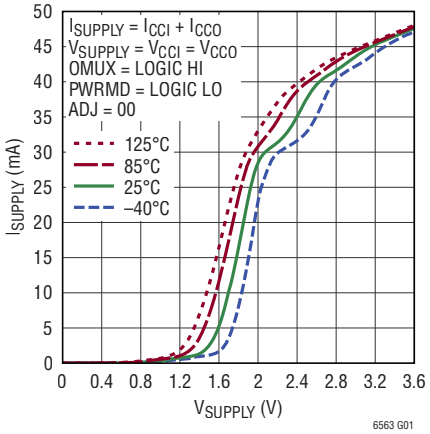
Note 4: HI pin voltage should be at least 0.2V higher than V_{CM}.

Note 5: This parameter is specified by design and/or characterization and is not tested in production.

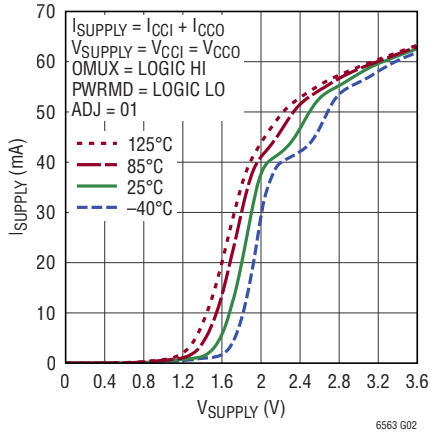
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V, and CM = 1.5V. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_{L_EXT} = 100Ω differential, OUT connected to TERM and $\overline{OUT}$ connected to $\overline{TERM}$.

I_{SUPPLY} vs V_{SUPPLY} Over Temperature



I_{SUPPLY} vs V_{SUPPLY} Over Temperature



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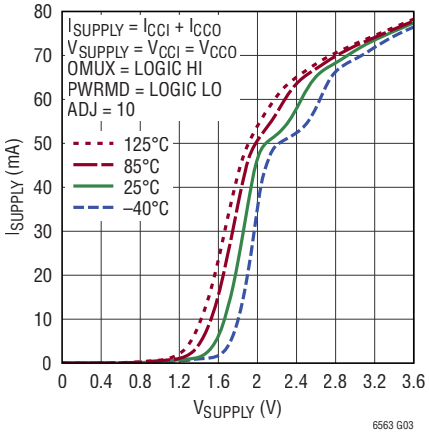
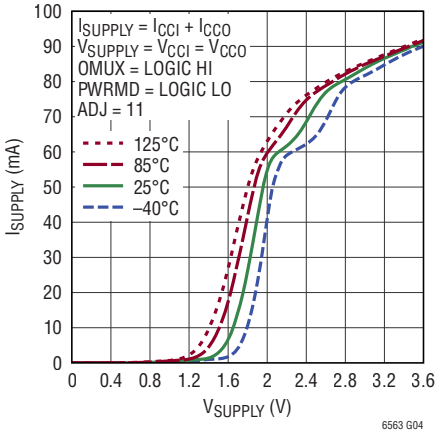
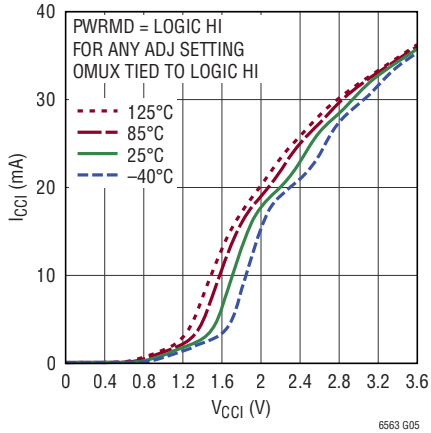


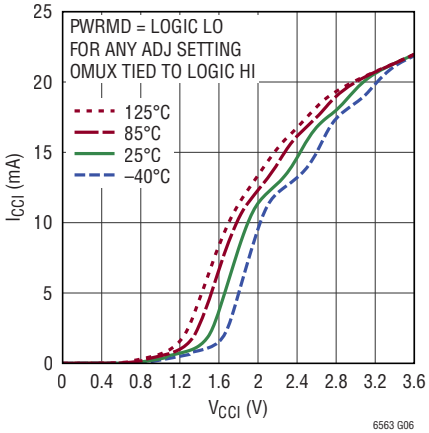
I_{SUPPLY} vs V_{SUPPLY} Over Temperature



I_{CCI} vs V_{CCI} Over Temperature



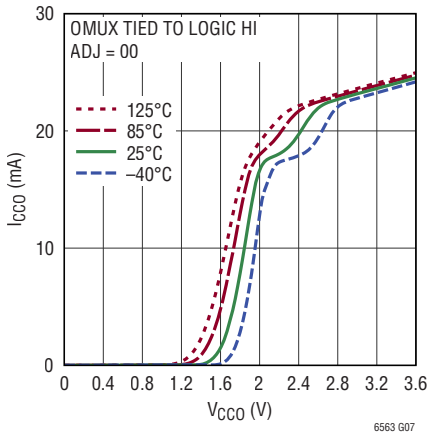
I_{CCI} vs V_{CCI} Over Temperature



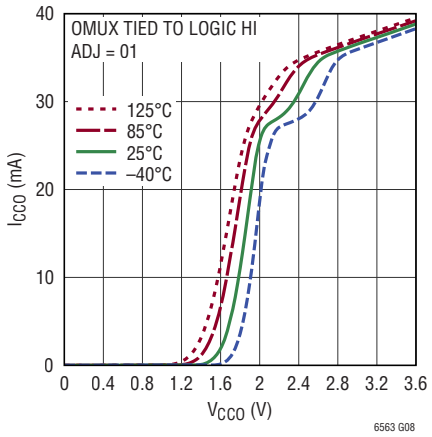
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V, and CM = 1.5V. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_{L_EXT} = 100Ω differential, OUT connected to TERM and $\overline{OUT}$ connected to $\overline{TERM}$.

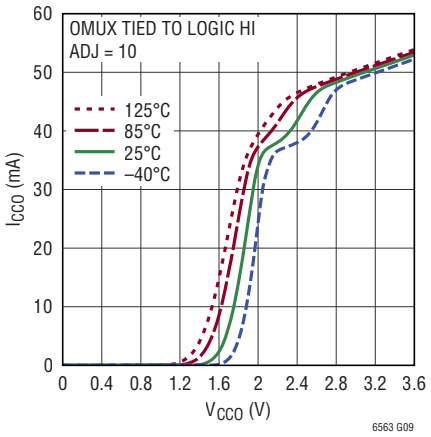
I_{CCO} vs V_{CCO} Over Temperature



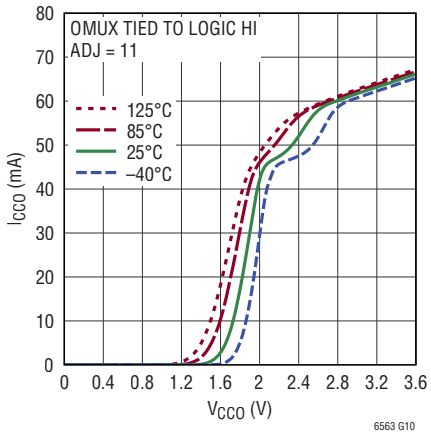
I_{CCO} vs V_{CCO} Over Temperature



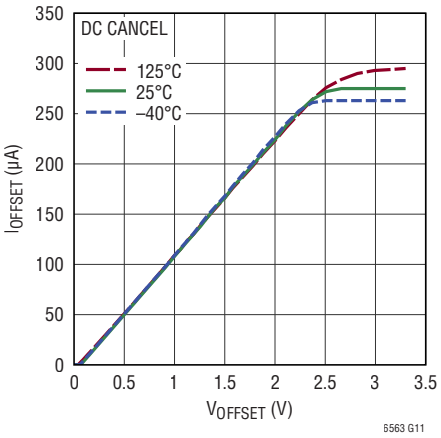
I_{CCO} vs V_{CCO} Over Temperature



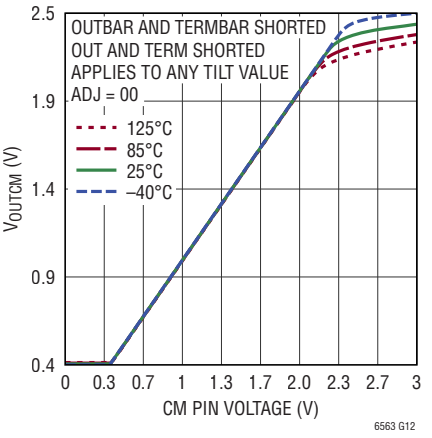
I_{CCO} vs V_{CCO} Over Temperature



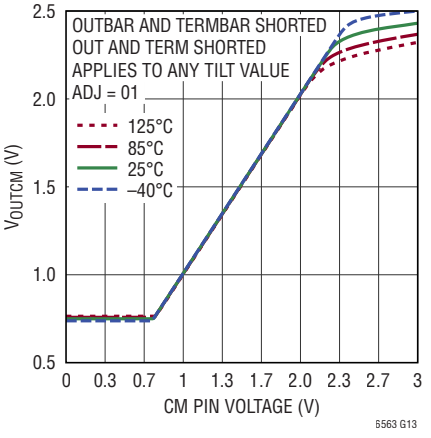
I_{OFFSET} vs V_{OFFSET}



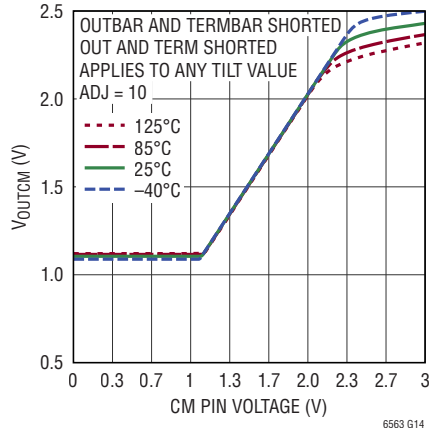
Output Common Mode Control



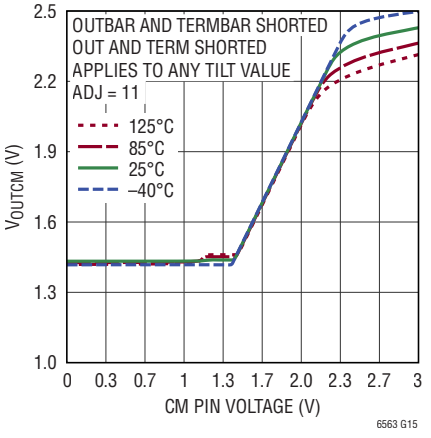
Output Common Mode Control



Output Common Mode Control



Output Common Mode Control



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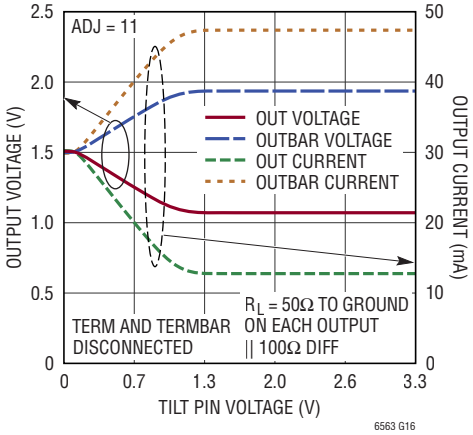
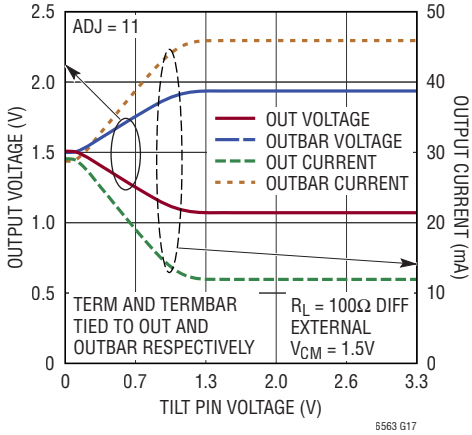
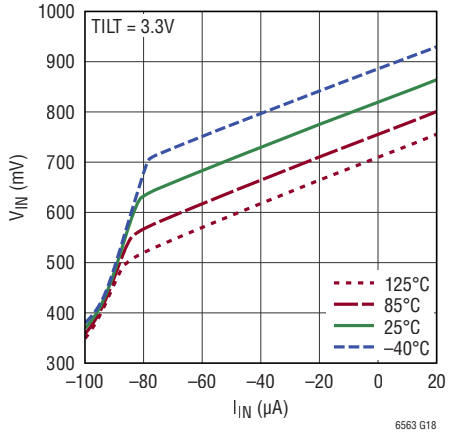
Output Tilt Control



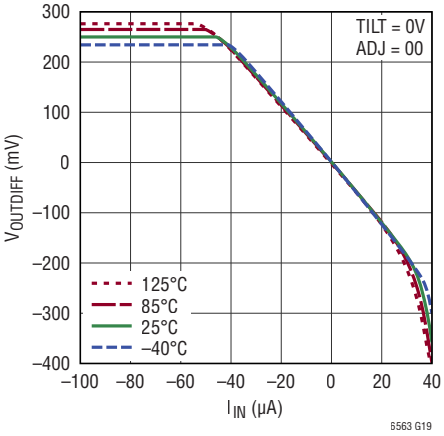
Output Tilt Control



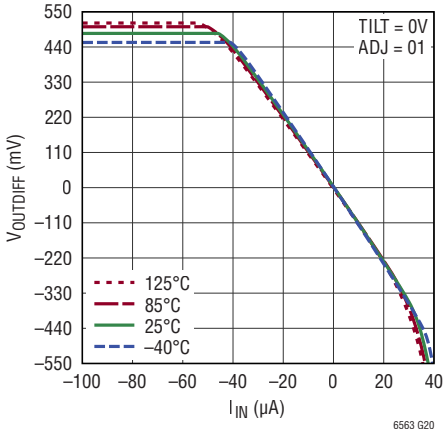
V_{IN} vs I_{IN} Over Temperature



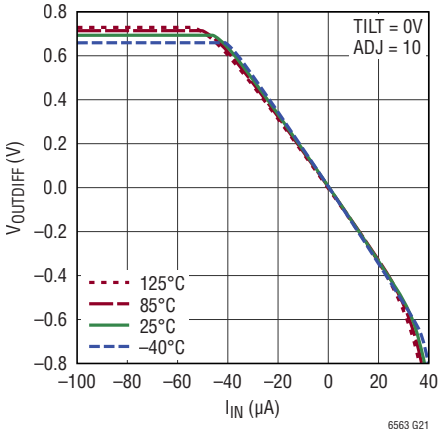
$V_{OUTDIFF}$ vs I_{IN} Over Temperature



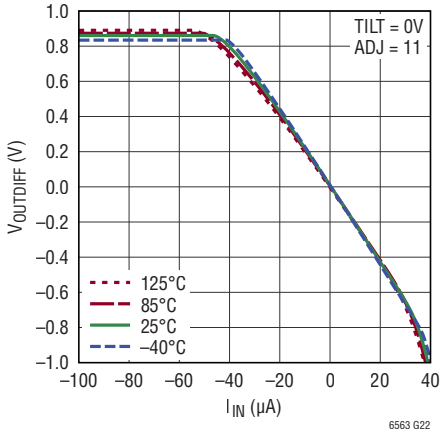
$V_{OUTDIFF}$ vs I_{IN} Over Temperature



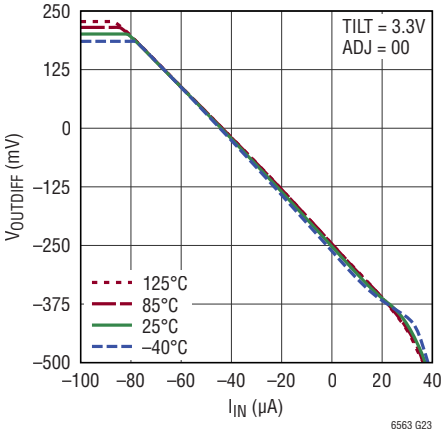
$V_{OUTDIFF}$ vs I_{IN} Over Temperature



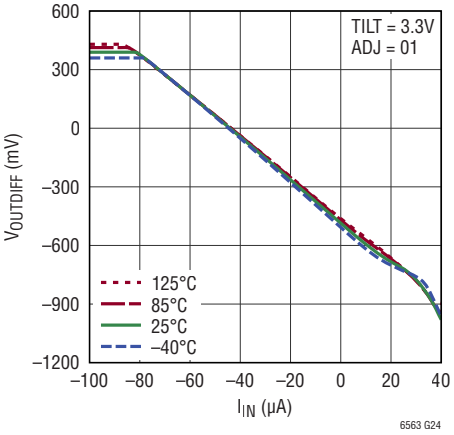
$V_{OUTDIFF}$ vs I_{IN} Over Temperature



$V_{OUTDIFF}$ vs I_{IN} Over Temperature



$V_{OUTDIFF}$ vs I_{IN} Over Temperature



Rev. 0

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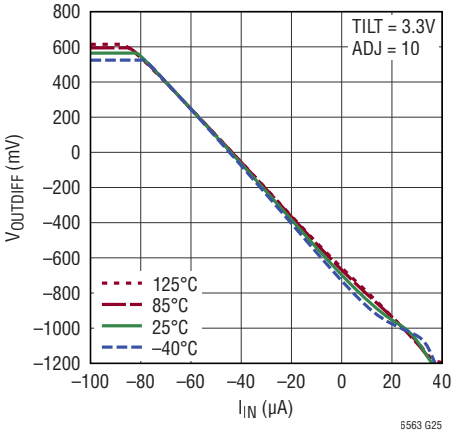
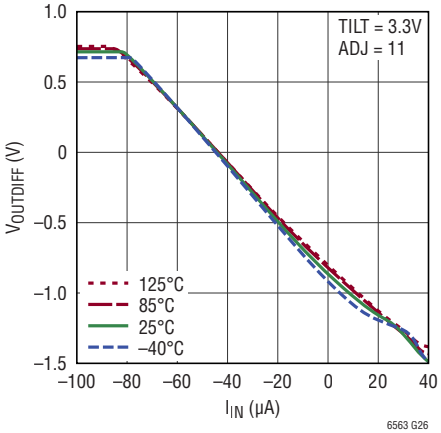
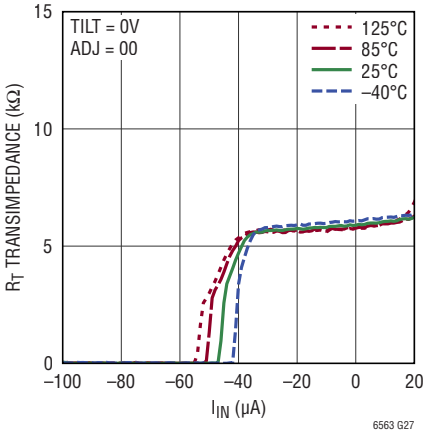
$V_{OUTDIFF}$ vs I_{IN} Over Temperature



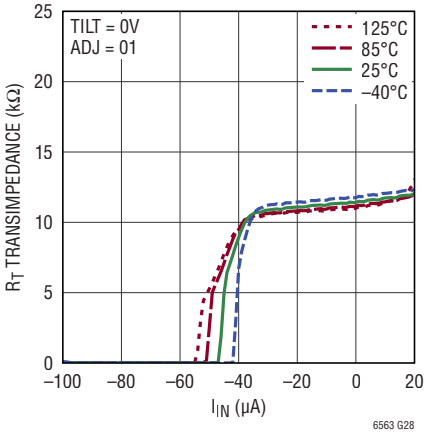
$V_{OUTDIFF}$ vs I_{IN} Over Temperature



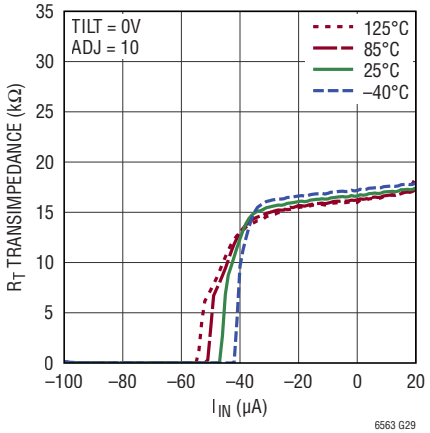
R_T Transimpedance vs I_{IN}



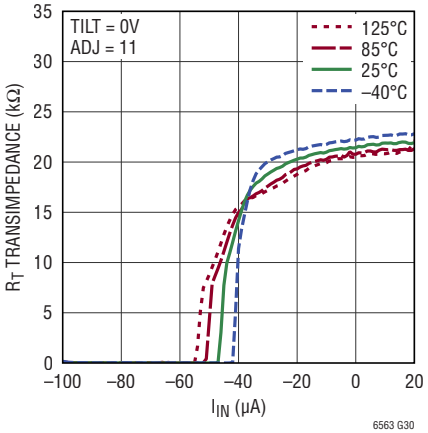
R_T Transimpedance vs I_{IN}



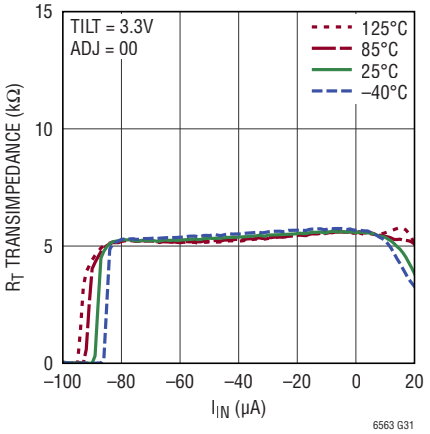
R_T Transimpedance vs I_{IN}



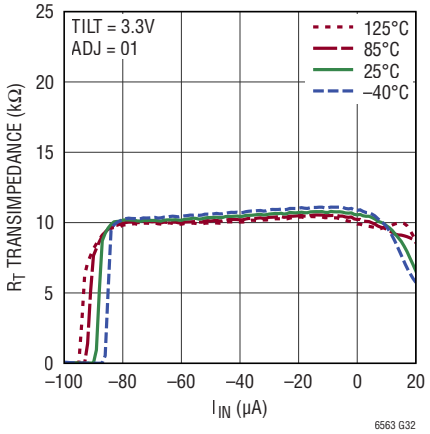
R_T Transimpedance vs I_{IN}



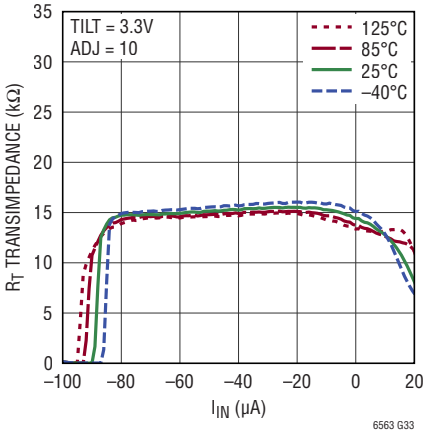
R_T Transimpedance vs I_{IN}



R_T Transimpedance vs I_{IN}



R_T Transimpedance vs I_{IN}



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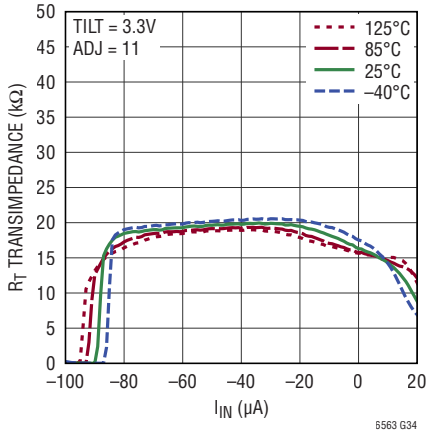
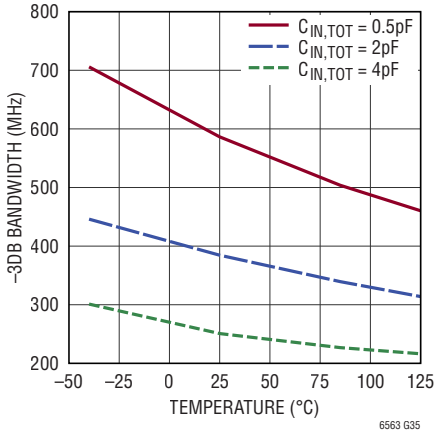
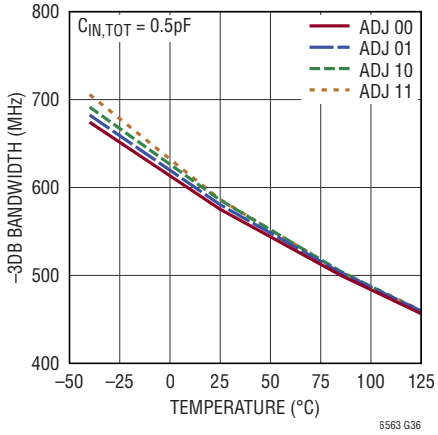
R_T Transimpedance vs I_{IN}



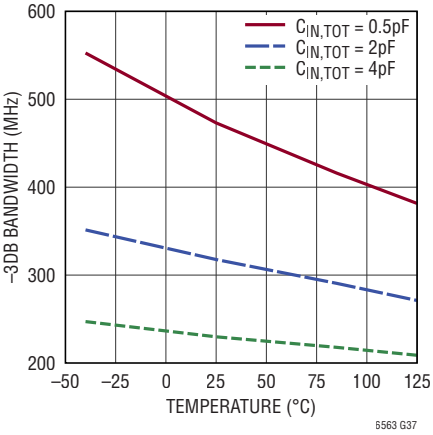
–3dB Bandwidth vs Temperature Over $C_{IN,TOT}$



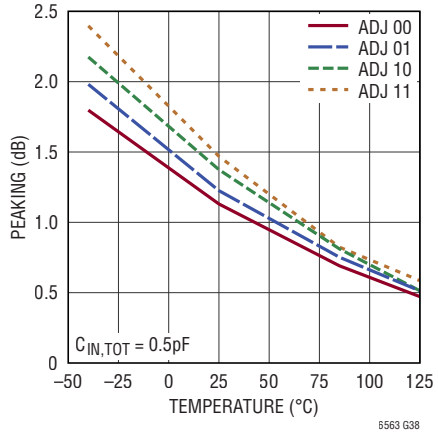
–3dB Bandwidth vs Temperature for Various ADJ Setttings



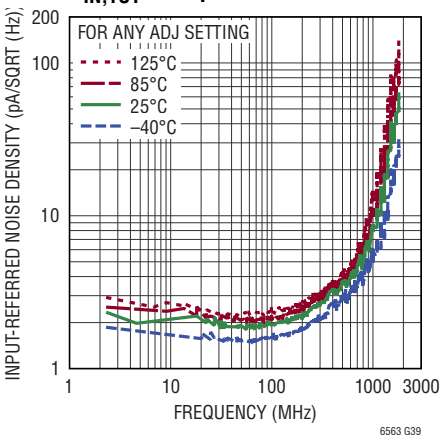
–3dB Bandwidth vs Temperature (Tilted) Over $C_{IN,TOT}$



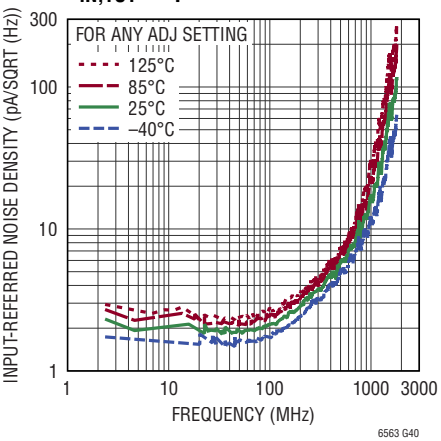
Peaking vs Temperature for Various ADJ Setttings



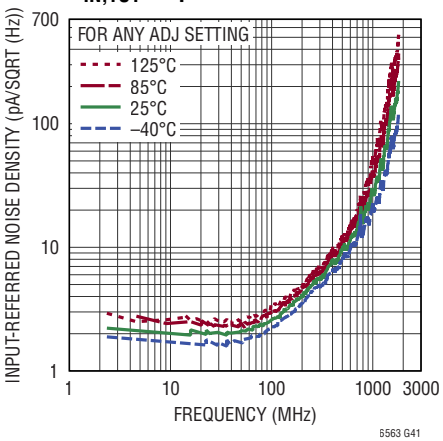
Input-Referred Noise Density with $C_{IN,TOT}$ = 0.5pF



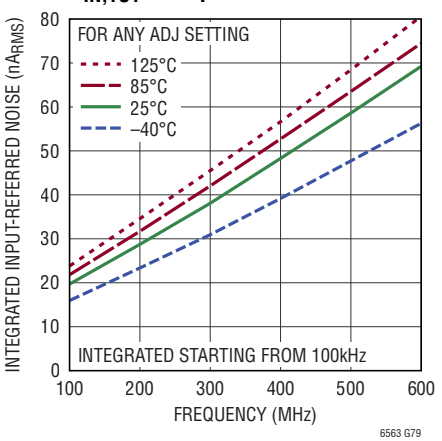
Input-Referred Noise Density with $C_{IN,TOT}$ = 2pF



Input-Referred Noise Density with $C_{IN,TOT}$ = 4pF



Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 0.5pF



Rev. 0

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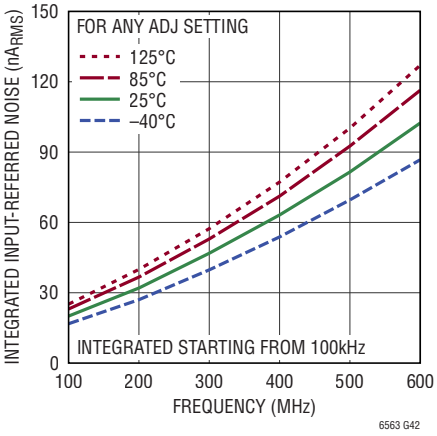
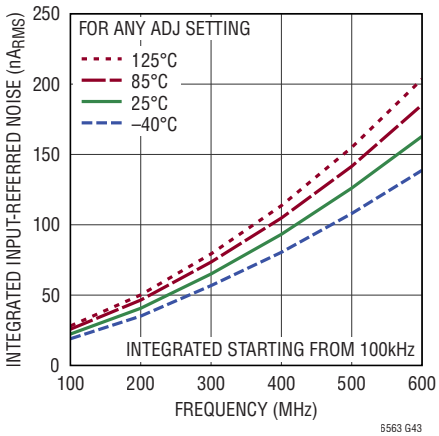
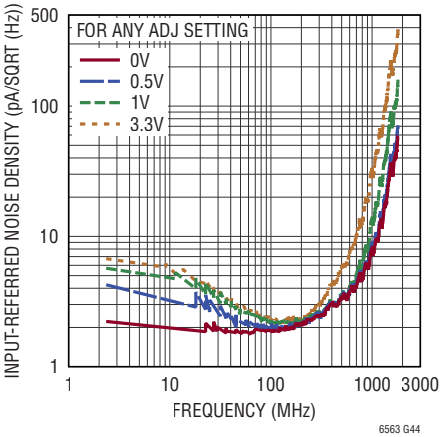
Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 2pF



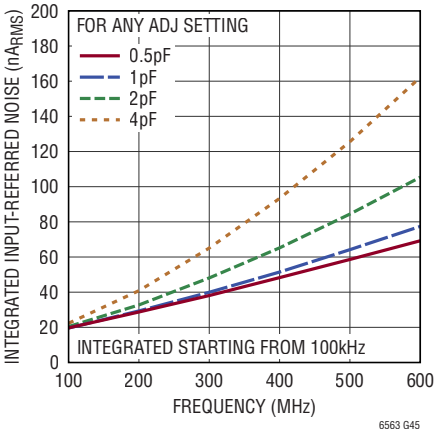
Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 4pF



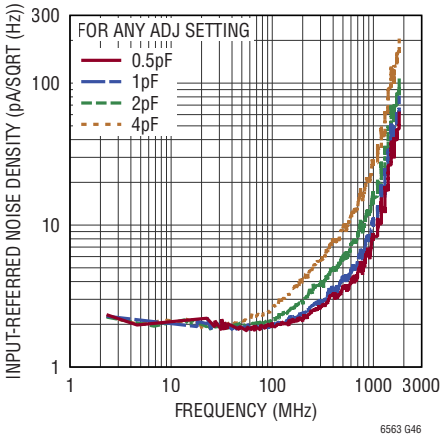
Input-Referred Noise Density for various Tilt Voltages with $C_{IN,TOT}$ = 0.5pF



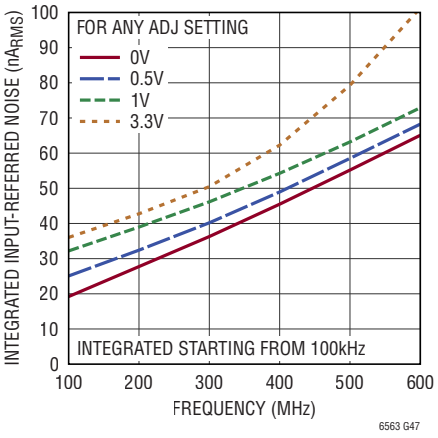
Integrated Input-Referred Noise vs Bandwidth for various $C_{IN,TOT}$



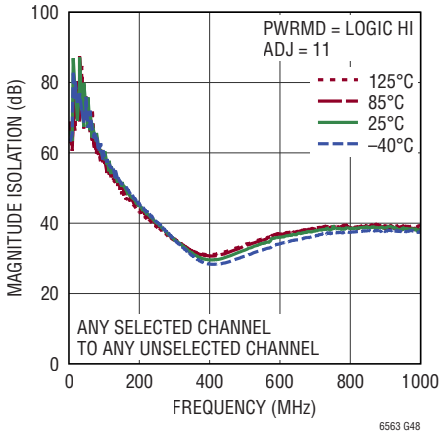
Input-Referred Noise Density for various $C_{IN,TOT}$



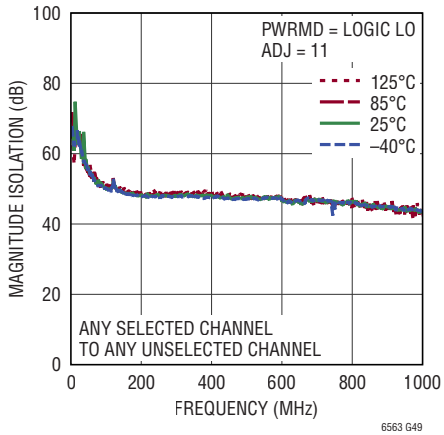
Integrated Input-Referred Noise for various Tilt Voltages with $C_{IN,TOT}$ = 0.5pF



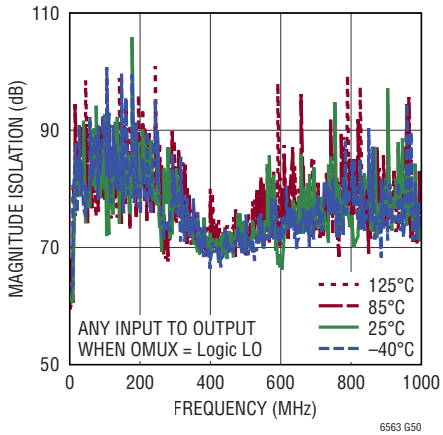
Channel to Channel Isolation vs Frequency Over Temperature



Channel to Channel Isolation vs Frequency Over Temperature



OMUX Isolation vs Frequency Over Temperature



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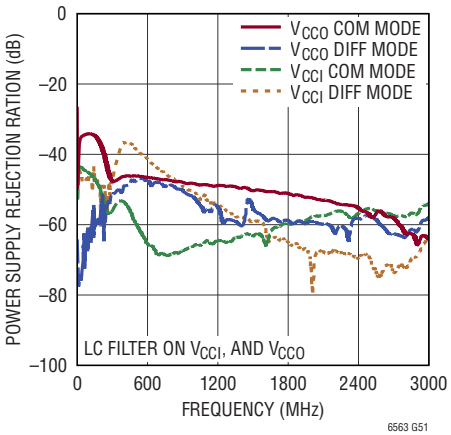
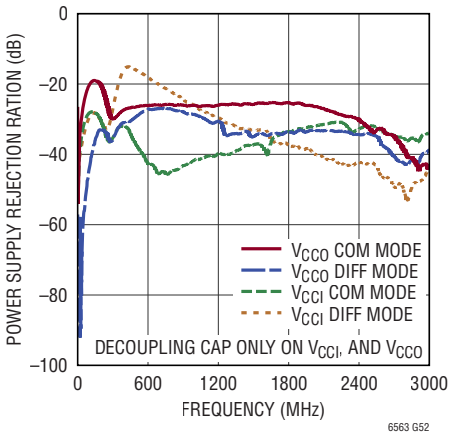
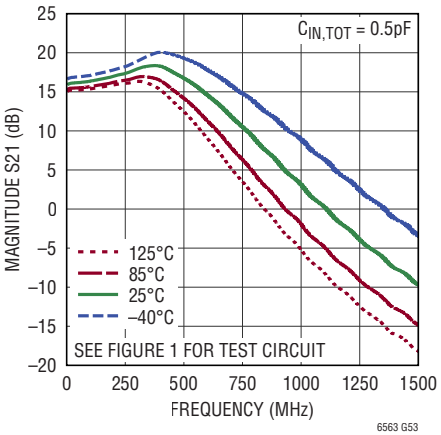
PSRR Out to V_{CCI}, V_{CCO}



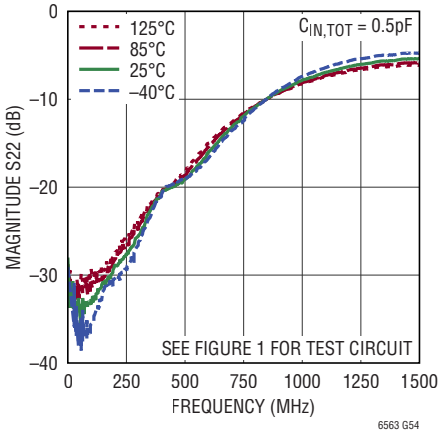
PSRR Out to V_{CCI}, V_{CCO}



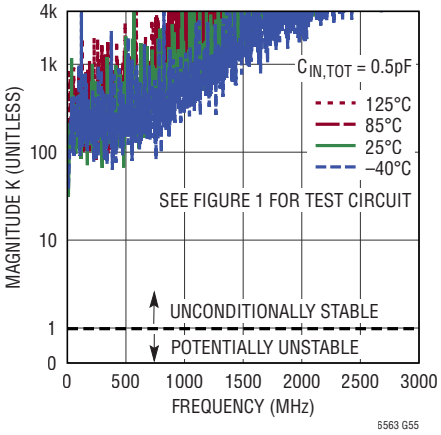
S21ds (Gain) vs Frequency Over Temperature



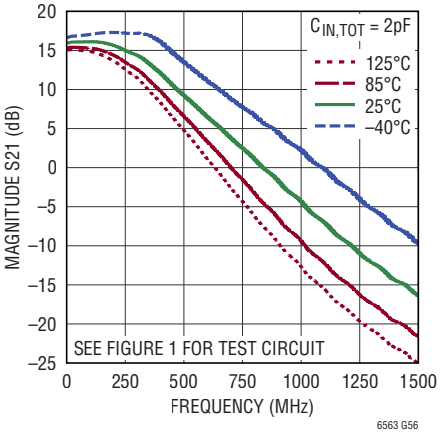
S22dd vs Frequency Over Temperature



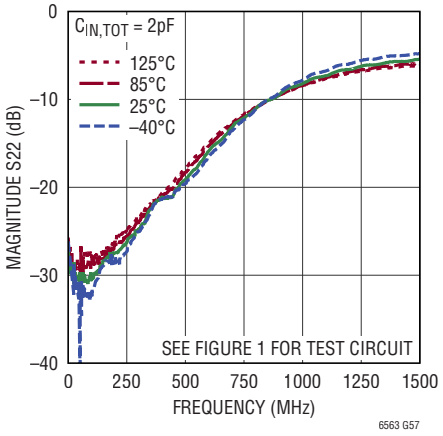
Stability Factor K vs Frequency Over Temperature



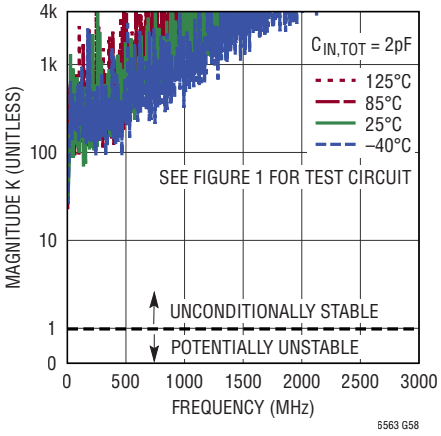
S21ds (Gain) vs Frequency Over Temperature



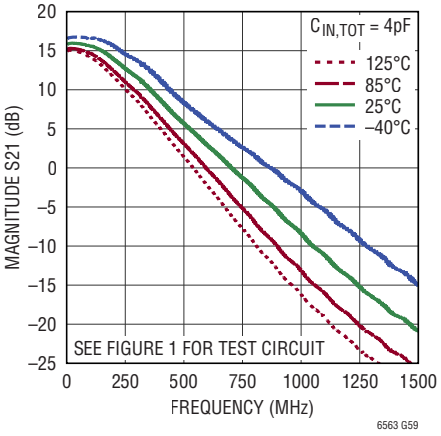
S22dd vs Frequency Over Temperature



Stability Factor K vs Frequency Over Temperature



S21ds (Gain) vs Frequency Over Temperature



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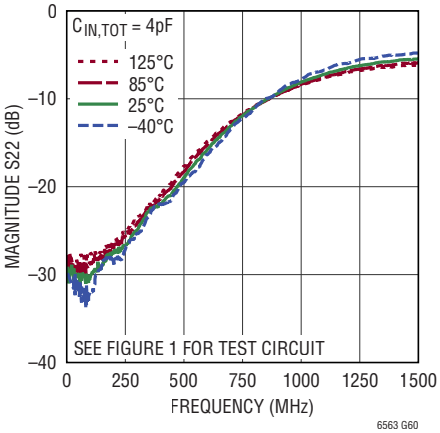
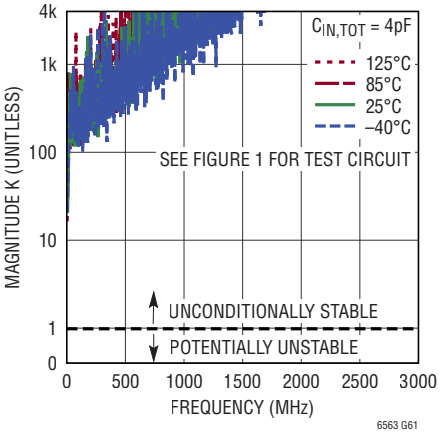
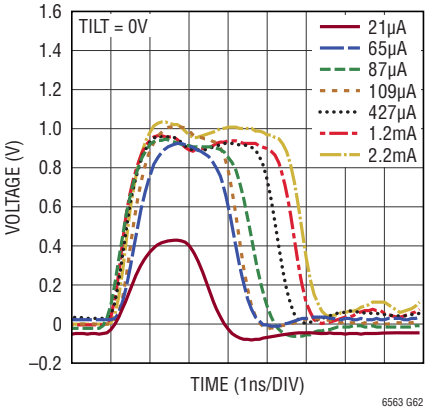
S22dd vs Frequency Over Temperature



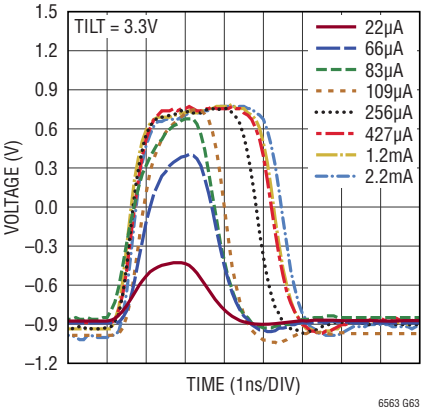
Stability Factor K vs Frequency Over Temperature



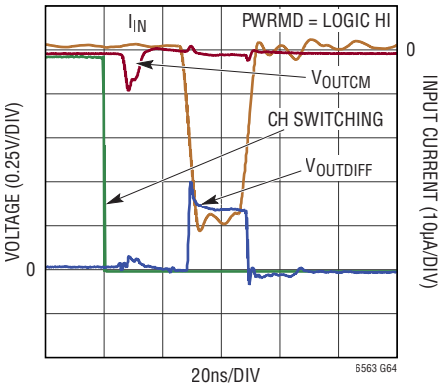
Pulse Response for Various I_{IN} $C_{IN,TOT}$ = 1pF, 2ns Pulse Width



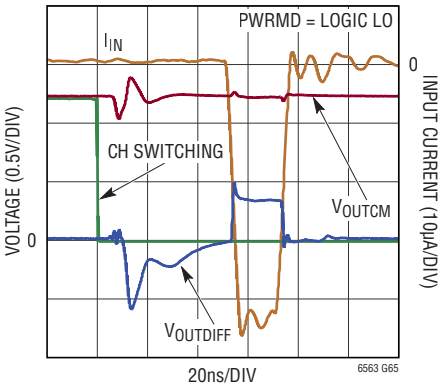
Pulse Response for Various I_{IN} $C_{IN,TOT}$ = 1pF, 2ns Pulse Width



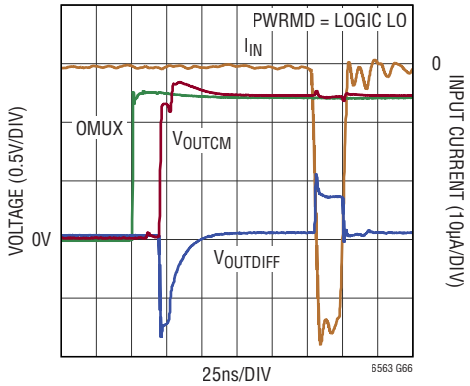
Channel Switching Time



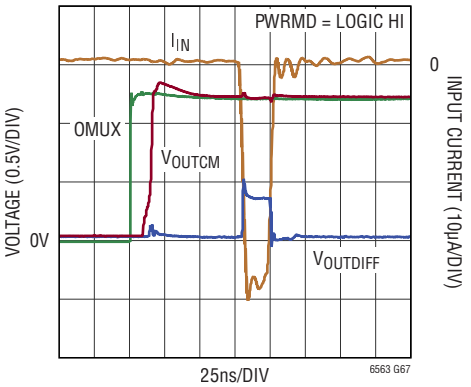
Channel Switching Time



OMUX Switching Time



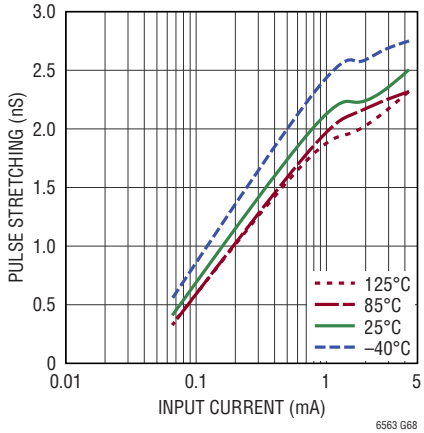
OMUX Switching Time



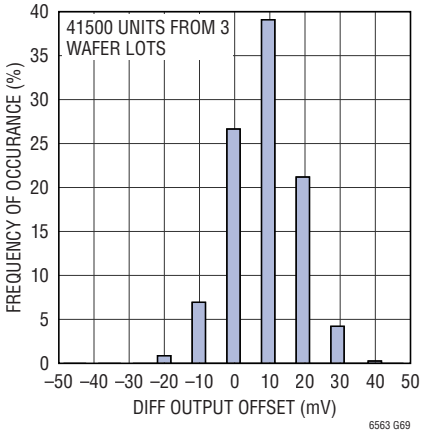
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V, and CM = 1.5V. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_{L_EXT} = 100Ω differential, OUT connected to TERM and $\overline{OUT}$ connected to $\overline{TERM}$.

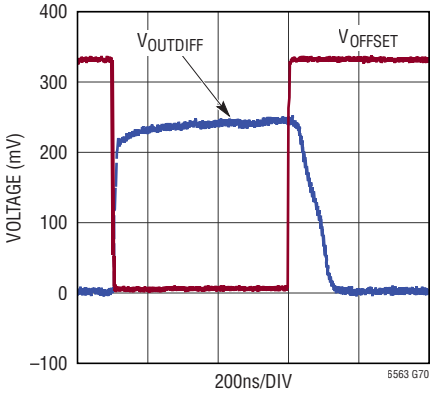
Pulse Stretching vs Input Current



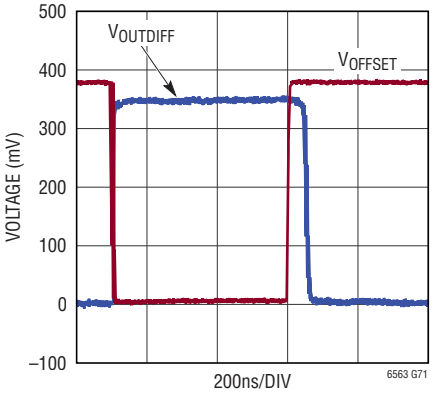
Output Offset Histogram



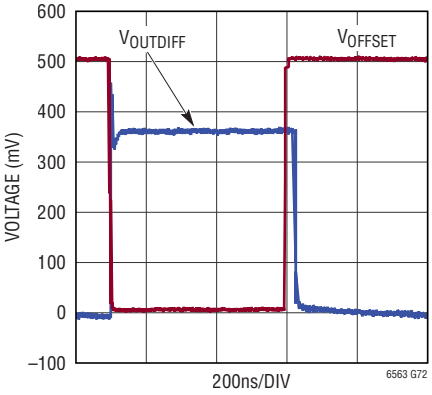
Output Response to V_{OFFSET} Pin Step



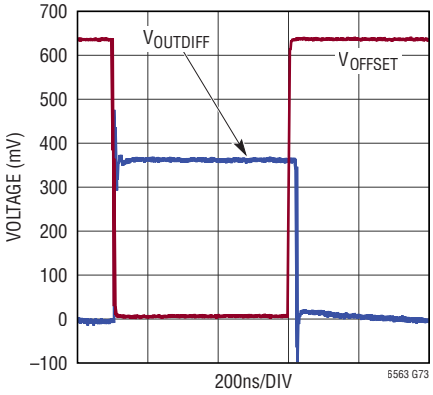
Output Response to V_{OFFSET} Pin Step



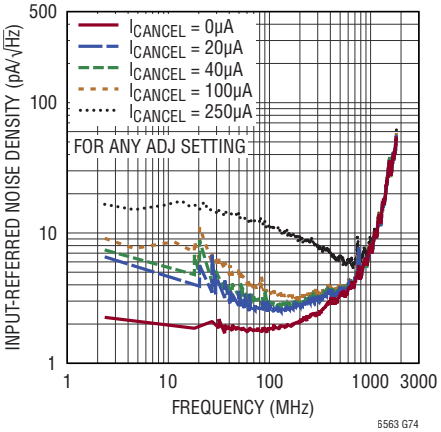
Output Response to V_{OFFSET} Pin Step



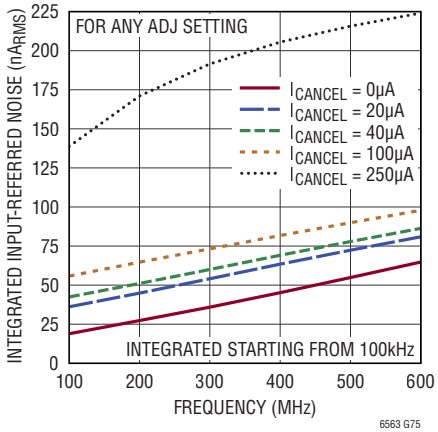
Output Response to V_{OFFSET} Pin Step



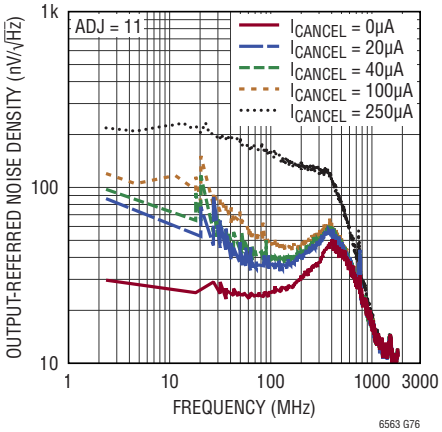
Input-Referred Noise Density for Various Input Current Cancellation with $C_{IN,TOT}$ = 0.5pF



Integrated Input-Referred Noise for Various Input Current Cancellation with $C_{IN,TOT}$ = 0.5pF

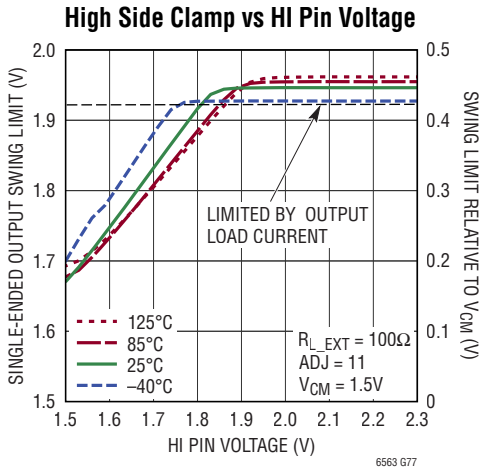


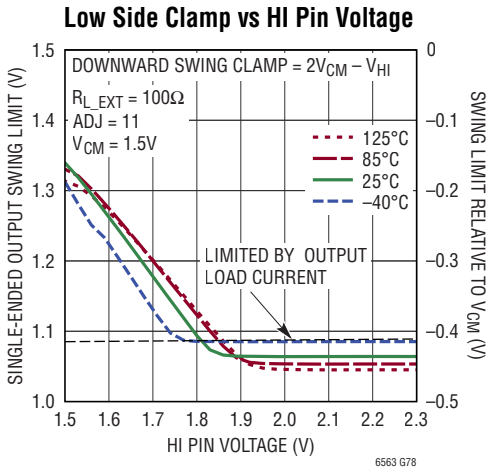
Output-Referred Noise Density for Various Input Current Cancellation with $C_{IN,TOT}$ = 0.5pF



TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at $\overline{CHSEL0}$ = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V, and CM = 1.5V. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_{L_EXT} = 100Ω differential, OUT connected to TERM and $\overline{OUT}$ connected to $\overline{TERM}$.





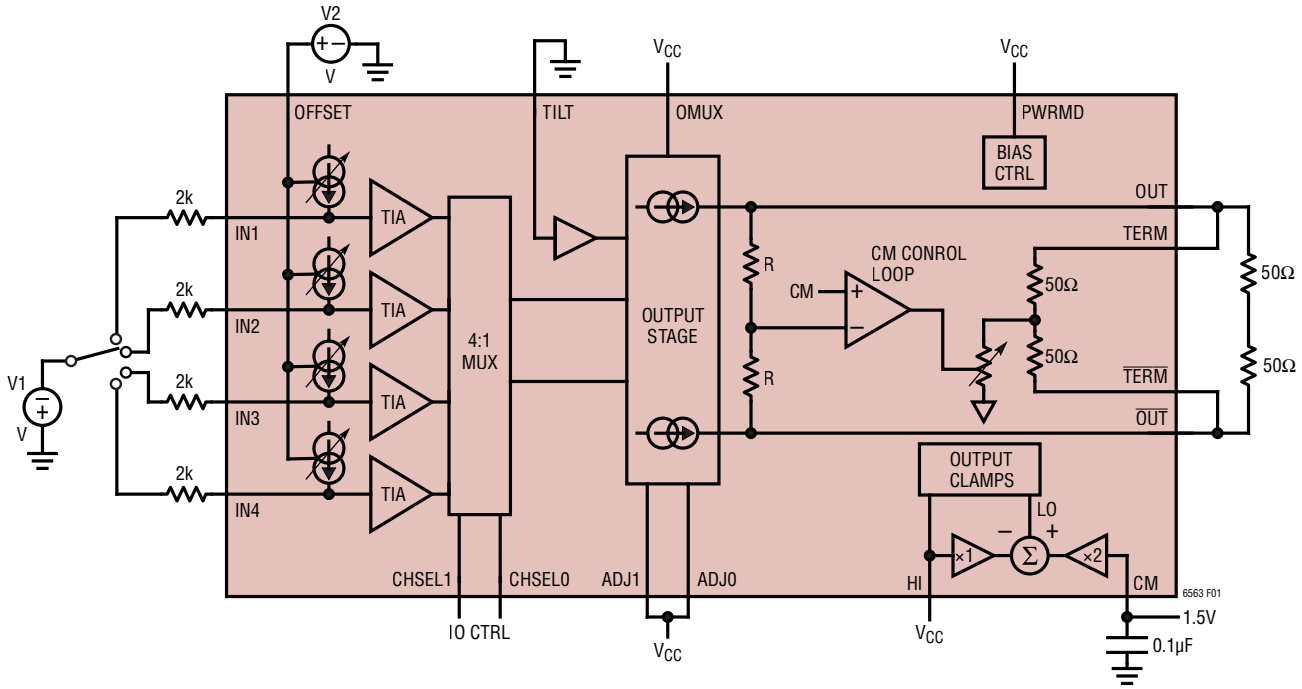


Figure 1. Electrical Characterization Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

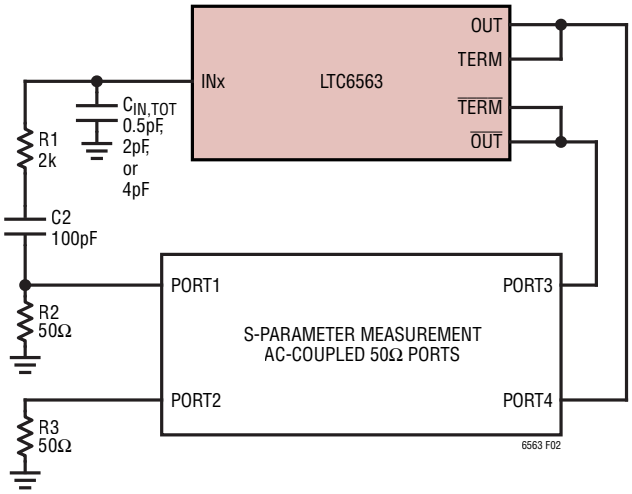


Figure 2. S-Parameters Test Circuit

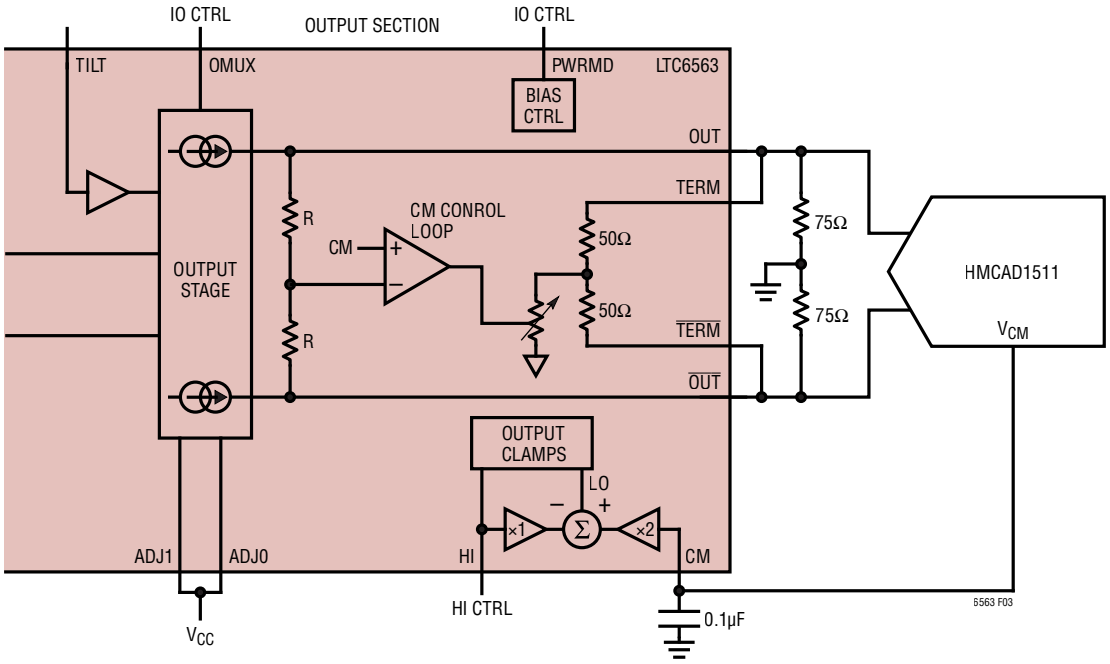


Figure 3. Driving HMCAD1511 (ADJ11, Tilt = 3.3V, CM = 0.9V, FS = 2.4V$_{P-P}$)

PIN FUNCTIONS

GND (Pins 1, 3, 18, 20, Exposed Pad Pin 25): Negative Power Supply. Normally tied to ground. All GND pins and the exposed pad must be tied to the same voltage. The exposed pad (pin 25) should have multiple via holes to the underlying ground plane for low inductance and good heat transfer.

IN4, IN1, IN2, IN3 (Pin 2, Pin 19, Pin 21, Pin 24,): Input pins for the transimpedance amplifier for channels 4, 1, 2, and 3 respectively. The active channel is internally biased to 0.8V. See the Applications Information section for specific recommendation.

PWRMD (Pin 4): Power mode is a CMOS input for controlling the power consumption. The PWRMD pin has a 208k internal pull-up resistor to V_{CCI}. Default value is 3.3V.

V_{CCI} (Pin 5): Positive power supply for the input stages. Typically, 3.3V. A series ferrite bead such as the MPZ1005A331ETD25 should be used and bypass capacitor of 680pF and 0.1µF should be placed as close to the part as possible between V_{CCI} and ground.

OMUX (Pin 6): Output MUX is a CMOS input for controlling the output multiplexing function. The OMUX pin has internal 208k pull-up resistor to V_{CCI}. Default value is 3.3V.

CM (Pin 7): Output Common Mode Reference Voltage. The voltage on this pin sets the output common mode voltage level. On a 3.3V supply, the CM pin floats to a default 0.9V. The CM pin has an input impedance of 16.3kΩ. The CM pin should be bypassed with a high-quality ceramic capacitor of at least 0.01µF.

HI (Pin 8): High Side Clamp Voltage. The voltage applied to the HI pin sets the upper voltage limit to $\overline{OUT}$ and OUT pins. The HI voltage also limits the lower voltage swing on both output pins to $2V_{CM}$ – HI, for symmetrical clamping around the CM voltage. On a 3.3V supply, the HI pin will float to a default 1.8V. The HI pin has an input impedance of 13.6kΩ. The HI pin should be bypassed with a high-quality ceramic capacitor of at least 0.01µF.

$\overline{OUT}$, OUT (Pin 9, Pin 12): Differential Output Pins. For voltage mode output, connect $\overline{OUT}$ to $\overline{TERM}$ and OUT to TERM. For current mode output or when using external load resistors, float $\overline{TERM}$ and TERM.

$\overline{TERM}$, TERM (Pin 10, Pin 11): Internal Termination. These pins have 50Ω load resistors coupled to GND and are intended to connect to the differential output pins.

CHSEL1, CHSEL0 (Pin 13, Pin 15): MSB and LSB for Channel Selection. These pins are CMOS inputs with internal 218k pull-down resistors to GND.

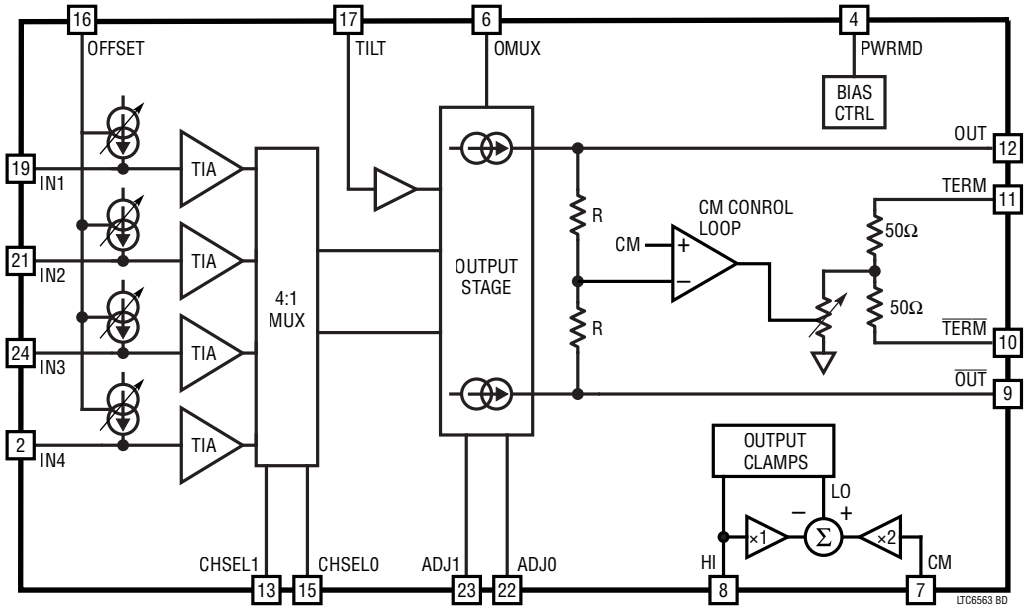
V_{CCO} (Pin 14): Positive power supply for the output stage. Typically, 3.3V. V_{CCO} can be tied to V_{CCI} for single supply operation. A series ferrite bead such as the MPZ1005A331ETD25 should be used and bypass capacitors of 680pF and 0.1µF should be placed as close as possible between V_{CCO} and ground.

OFFSET (Pin 16): Input Offset Adjust. This pin accepts a voltage input that controls current sources on each input pin. These current sources can be used to cancel DC currents flowing into the detector. The OFFSET pin has an internal pull-down resistor to GND.

TILT (Pin 17): Output Differential Offset. The voltage on this pin controls the outputs' differential offset. The TILT pin has an internal 22.7k pull-down resistor to GND.

ADJ0, ADJ1 (Pin 22, Pin 23): LSB and MSB for output gain and current adjusts. The adjust pins set the output stage quiescent current and current gain. See Applications Information section to optimize the ADC interface. These pins are CMOS inputs with internal 218k pull-down resistors to GND.

BLOCK DIAGRAM



OPERATION

The LTC6563 is a four channel transimpedance amplifier with an integrated 4-to-1 multiplexer and ADC driver stage. Each of the transimpedance amplifiers converts an input current to an output voltage. The integrated 4:1 multiplexer simplifies the system design while saving space and power. In addition, output multiplexing is possible by using the OMUX pin. This allows multiple 4-channel LTC6563 devices to be combined. 8, 12, 16 … 32 input channels are easily multiplexed into a single differential output.

The LTC6563 is optimized to drive high speed differential input analog-to-digital converters (ADCs). $\overline{OUT}$ and OUT have single-ended swings from as low as about 180mV to about V_{CCO} – 1V. The LTC6563 provides four modes of output drive for matching input swing of high-speed ADCs.

The tilt feature allows the output stage to offset to take advantage of the full differential input range of the ADCs. The outputs have programmable clamps that limit the output swing in saturation events. These clamps provide protection to the front end of the ADC. The HI pin sets the maximum swing, while a symmetric minimum swing limit is set up internally.

In typical LIDAR applications, the LTC6563 amplifies the output current of an APD. APD are biased near breakdown to achieve high current gain. Under intense optical illumination, they can conduct large currents, often in excess of 1A. The LTC6563 survives and quickly recovers from large overload currents of this magnitude. During recover, any TIA is blinded from subsequent pulses. The LTC6563 recovers from 1mA saturation events in less than 2.5ns without phase reversal, minimizing this form of data loss.

Ambient light is problematic for LIDAR receiver chains. The DC current can easily saturate the linear range of any TIA. The LTC6563 provides a control for DC cancelation to the inputs and can cancel up to 200µA of DC current. The DC cancelation is designed to minimizing additive noise.

APPLICATIONS INFORMATION

Output Offset and Current Control

The output stage of the LTC6563 has many options. The ADJ1 and ADJ0 pins provide four options for the output current drive. The output voltage swing is dependent on the adjust setting, the external differential termination resistor, and the Tilt input. The purpose of the Tilt input is to offset the DC output voltages, thereby increasing the full output swing of the TIA for unipolar inputs. Output TILT is essential for the ADC as the input from the photodetector is unipolar. To maximize the input swing of the ADC, the DC value of OUT is offset low while the DC value of OUT is offset high. This allows the LTC6563 to maximize the full dynamic range of the ADC. These pins should be connected to low noise inputs.

LTC6563 transimpedance gain (RT) consists of the overall gain from the multi-stages involved in producing the output for a given input current. The output is differential and ½ RT is achieved if only one of the outputs is utilized.

It is possible to change the transimpedance gain (RT) by changing R_{L_EXT} as shown in Table 1, and Table 2. Also, since the ADJ pins respond in less than 100ns, these pins can be used for on the fly gain switching if the application needs that. An example would be to reduce the TIA gain if an overly strong signal is received by the LTC6563. It's important to note the following regarding gain adjustment:

- The linear input current range (40µA with no Tilt, 90µA with full Tilt) is not affected by these changes.
- R_{LDIFF} refers to the total load seen by the differential output(s) whereas R_{L_EXT} is the external differential load. Refer to Figure 17 to Figure 19 to see examples of various external single-ended load (50Ω, 75Ω, and 100Ω) illustrated.

Table 1. Output Stage when Tilt Pin = 0V, OUT Connected to TERM and $\overline{OUT}$ Connected to $\overline{TERM}$[1]

IIN (µA)	ADJ1	ADJ0	OUT (mA)	OUTBAR (mA)	R_T (Ω) R_{L_EXT} = 100Ω DIFF	R_T (Ω) R_{L_EXT} = 200Ω DIFF	R_T (Ω) R_{L_EXT} = OPEN
0	0	0	7	7	5.55k	7.4k	11.1k
	0	1	14	14	11.1k	14.8k	22.2k
	1	0	21	21	16.65k	22.2k	33.3k
	1	1	28	28	22.2k	29.6k	44.4k
45	0	0	12	2	5.55k	7.4k	11.1k
	0	1	24	4	11.1k	14.8k	22.2k
	1	0	36	6	16.65k	22.2k	33.3k
	1	1	48	8	22.2k	29.6k	44.4k

[1] Output voltage compliance to be observed at higher R_{L_EXT} and higher ADJ settings.

Table 2. Output Stage when Tilt Pin = V_{CC}, OUT Connected to TERM and $\overline{OUT}$ Connected to $\overline{TERM}$[1]

IIN (µA)	ADJ1	ADJ0	OUT (mA)	OUTBAR (mA)	R_T (Ω) R_{L_EXT} = 100Ω DIFF	R_T (Ω) R_{L_EXT} = 200Ω DIFF	R_T (Ω) R_{L_EXT} = OPEN
0	0	0	2	12	5.55k	7.4k	11.1k
	0	1	4	24	11.1k	14.8k	22.2k
	1	0	6	36	16.65k	22.2k	33.3k
	1	1	8	48	22.2k	29.6k	44.4k
90	0	0	12	2	5.55k	7.4k	11.1k
	0	1	24	4	11.1k	14.8k	22.2k
	1	0	36	6	16.65k	22.2k	33.3k
	1	1	48	8	22.2k	29.6k	44.4k

[1] Output voltage compliance to be observed at higher R_{L_EXT} and higher ADJ settings.

APPLICATIONS INFORMATION

- Increasing R_{LDIFF} slightly reduces the signal bandwidth.
- Output voltage compliance ($V_{COMPLIANCE}$) to be observed relative to R_{LDIFF} , ADJ settings, and CM voltage . Here is an example where output voltage compliance is violated:

  R_{LDIFF} = 100Ω, Tilt = V_{CC}, ADJ1 = 1, ADJ0 = 0, CM = 1.7V, I_{IN} = 90µA

  Output Voltage (max) =

$$V_{CM} + \frac{|I_{OUT} - I_{OUTBAR}|}{2} \bullet \frac{R_{LDIFF}}{2}$$

Referring to Table 2 to read output current values:

Output Voltage (max) =

$$1.7V + \frac{|36mA - 6mA|}{2} \bullet \frac{100\Omega}{2} = 2.45V!$$

The maximum output voltage must remain below V_{CCO} – 1V (~2.3V) to comply with the $V_{COMPLIANCE}$ rating. Possible remedies are reducing output current(s) by using lower power ADJ settings, reducing the input APD current, reducing the differential load, or reducing the CM voltage.

Power Considerations

The LTC6563 has many power modes of operation. The state of the PWRMD, OMUX and ADJ pins will dictate the amount of current the LTC6563 will draw. Multiple power modes are offered to allow the user to select the appropriate one based upon the application while minimizing power dissipation.

Coupling the TIA Input – AC vs DC

Although the LTC6563 can AC-couple to the detector, best performance is achieved when DC-coupled to a negatively biased APD. DC-coupling reduces component count while allowing a DC current path from the APD. The LTC6563 OFFSET feature is designed to cancel DC currents. The maximum performance for switching speeds and saturation recovery occurs in this DC-coupled configuration.

When AC-coupling to the TIA input, R_B, is needed to establish a bias point for the detector. It is worth noting that R_B is a parallel path with the TIA for the APD current to flow through and it will impact the effective signal chain output gain.

This value of the biasing resistor and AC-coupling capacitor, C_{AC}, can potentially create a long time-constant. C_{AC} is chosen based on the reactance at the frequency of interest. However, R_B ideally should be large to avoid stealing

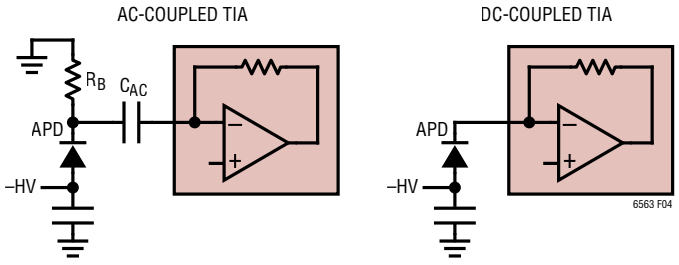


Figure 4. AC-Coupled Detector Circuit

Table 3. LTC6563 Power Dissipation Modes. X = Don't Care

PWRMD	OMUX	ADJ1	ADJ0	I_{VCCI} (mA)	I_{VCCO} (mA)	I_{TOTAL} (mA)	DESCRIPTION
0	0	X	X	4.5	0.1	4.6	LTC6563 shutdown.
0	1	0	0	21	24.5	45.5	LTC6563 enabled, non-selected inputs powered down, CM pin control disabled. This setting appropriate for a Responder device in a multi-chip/ multi-channel application.
0	1	0	1	21	38	59	
0	1	1	0	21	51.5	72.5	
0	1	1	1	21	64.5	85.5	
1	0	X	X	35	0.1	35.1	LTC6563 deselected (outputs stage off), non-selected inputs powered up.
1	1	0	0	34	24.5	58.5	LTC6563 enabled, non-selected inputs powered up, CM pin control active in setting output CM voltage. This setting appropriate for a Controller device in a multi-chip/multi-channel application.
1	1	0	1	34	38	72	
1	1	1	0	34	51.5	85.5	
1	1	1	1	34	64.5	98.5	

APPLICATIONS INFORMATION

current from the TIA path from APD signal. On one hand large R_B causes large RC time constants, while low R_B reduces the effective gain of the APD.

Another negative impact of this RC network is in the case for saturation events. When a large signal is received from the APD, this event will charge C_{AC}. This will negatively move the input bias of the TIAs and change the TIAs input impedance to transimpedance 14kΩ. This 14kΩ coupled with R_B and C_{AC} time constant will add the saturation recover time. Practical values of 100pF C_{AC} and R_B of 2.2kΩ will have large saturation recovery times >1µs with >50mA input signals. This effectively blinds the signal chain for the next input signal.

Channel Selection

There are four TIA inputs to the LTC6563. The active channel is selected using two channel selection bits CHSEL0 and CHSEL1. When a channel is changed and PWRMD is high, an output glitch takes <10ns to settle. When PWRMD is low and a channel is changed, an output glitch takes <500ns to settle. Inactive channels have 30dB of channel to channel isolation at 400MHz when PWRMD pin is high. When PWRMD is low the channel isolation is increased to more than 48dB.

Table 4. Channel Selection

CHSEL1	CHSEL0	OMUX	ACTIVE CHANNEL
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4
X	X	0	Hi-Z

DC Input Cancelation

The LTC6563 features a voltage controlled current source for DC input current cancelation with minimal noise impact. Identical currents are applied to each TIA input. The maximum current cancelation is 200µA. The OFFSET pin was designed to accommodate external closed loop design for fast settling and fast switching times. See I_{OFFSET} vs V_{OFFSET} curve for the transfer function. It is recommended to use a high-speed DAC to control the OFFSET pin.

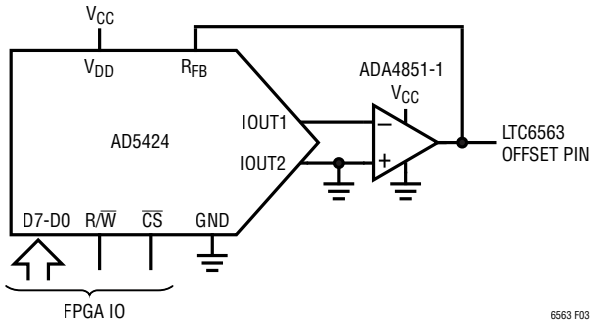


Figure 5. Recommended DC Cancel Circuit

Output MUXing

Refer to Figure 6 schematic. The output multiplexing (OMUX) requires at least one additional LTC6563 devices to operate in a Controller/Responder relationship. To multiplex multiple LTC6563's they need to share a DC connection at their outputs. The controller LTC6563 (U1) output stage needs to be connected to the internal termination resistors. For the CM control to function, the controller PWRMD pin must remain HIGH during the time any of the inputs of all the parallel network are enabled. That is because the CM servo loop is disabled if PWRMD is deasserted (low). The controller LTC6563 output circuit (U1) will control the common mode for all the multiplexing. All CM pins (U1-U4) are to be connected to the common mode of the ADC. If the output clamping feature (HI pin) is implemented, all CM pins (U1-U4) need to be connected to the same voltage for proper operation. Also, tie all HI pins (U1-U4) together and apply the required clamping voltage to them. The HI pin is used to set the high side clamp voltage at outputs. Internal circuity generates a symmetric low side clamp voltage with respect to the common mode voltage V_{CM}.

Maximum output high side voltage = HI pin voltage

Minimum output low side voltage = $V_{CM} – (HI – V_{CM}) = 2V_{CM} – HI$

Setting the Output CM Voltage

The LTC6563 can set the output Common Mode (CM) voltage using the CM input pin provided on the device.

APPLICATIONS INFORMATION

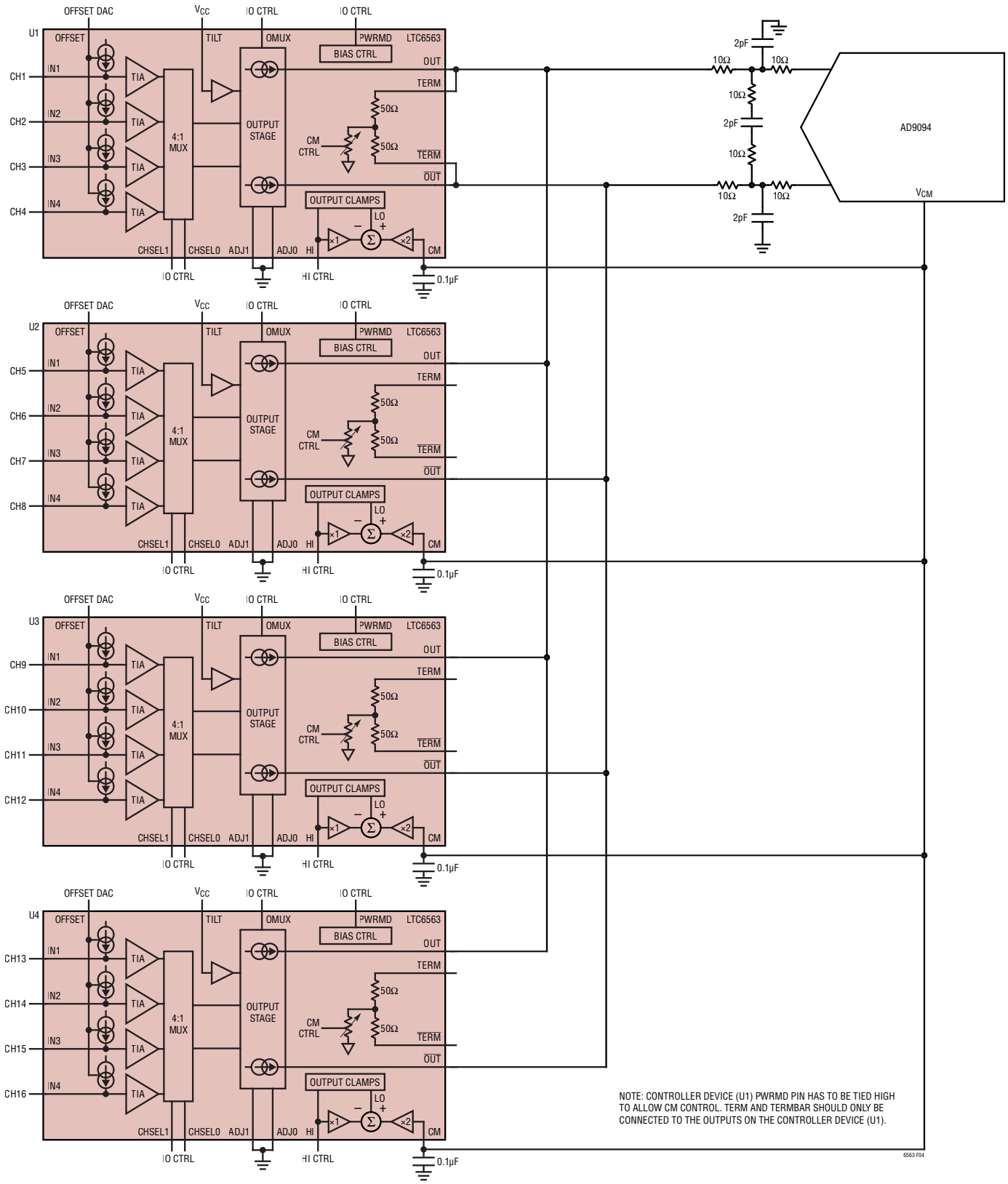


Figure 6. Typical Application with Multiplexed Outputs

APPLICATIONS INFORMATION

In applications where the LTC6563 is to drive an ADC, this is useful in matching the TIA output(s) to the ADC analog input CM. This effectively eliminates the need for a separate ADC-driver which saves cost, power, as well as board complexity and real estate.

The CM servo loop operates by varying the CM CTRL variable resistor internal to the LTC6563 such that V_{CMO}, average of V_{OUT} and V_{OUTBAR} voltages or $(V_{OUT} + V_{OUTBAR})/2$, matches the voltage applied to the CM. The loop will NOT function unless two conditions are met:

1. PWRMD must be set HI to activate the CM circuit.
2. OUT and $\overline{OUT}$ must have a DC connection to TERM and $\overline{TERM}$ respectively.

The internal 50Ω resistor(s) on the TERM and $\overline{TERM}$ pins provide a current path for CM servo functionality and serve as the load for the LTC6563's current mode output. Driving 50Ω terminated transmission lines or other impedance-matched loads is easily done using these internal resistors.

When using the output MUXing capability with multiple LTC6563's, such as the schematic shown in Figure 6, only one pair of TERM and TERMBAR pins should be connected to the OUT and $\overline{OUT}$. The device with the connected TERM and $\overline{TERM}$ will then set the CM for the MUX'ed devices.

Determining the CM Range

CM servo loop's voltage range is easily calculated using Ohm's law, as the output circuit can be described as a pair of current sources and a resistor network (see Figure 8). The amount of current supplied by the OUT and $\overline{OUT}$ current sources is determined by the ADJ setting, and the impedance at the output pins is determined by the internal and external resistor networks. These factors will determine the range of possible DC voltages at the outputs.

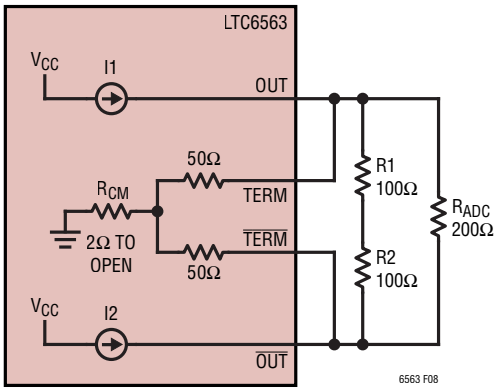


Figure 8. Equivalent Circuit for Driving an ADC with no GND (CM Referenced) External Load

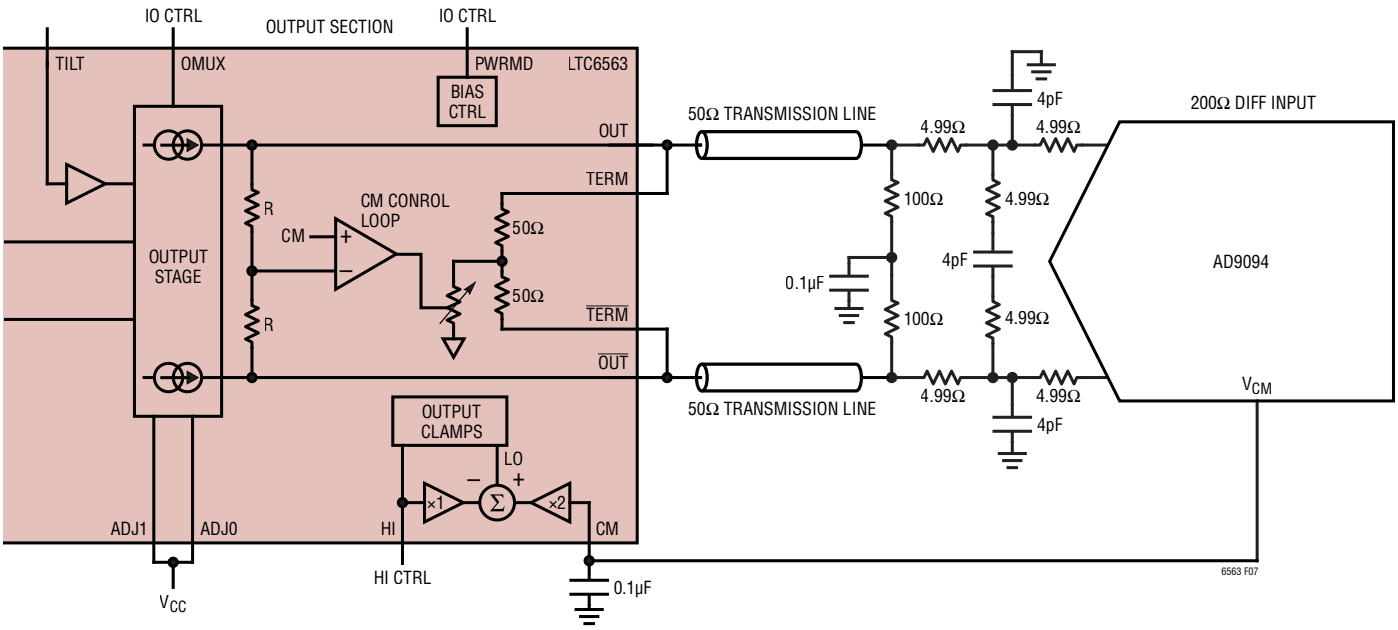


Figure 7. Typical Connection for CM Control/ADC Driving

APPLICATIONS INFORMATION

In order to simplify the analysis, an intuitive way to look at the output loading is to examine its equivalent half-circuit as shown in Figure 9. With the half-circuit method, any impedance that is shared between the two halves appears as double its original value (e.g. R_{CM} appears as $2 \bullet R_{CM}$ below).

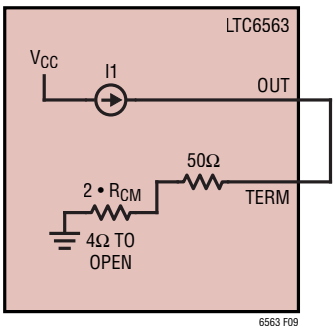


Figure 9. CM Half-Circuit Equivalent for a Non-Grounded External Load

The internal CM CTRL resistance varies from about 2Ω to essentially an open circuit. At the lower end of the CM CTRL resistance, R_{CM}, the output CM voltage will be at the minimum it can reach. And at the higher end of R_{CM}, it will be at the maximum it can reach.

The external CM resistance can also vary greatly, depending on whether any external loads are terminated differentially or to GND.

Detailed Example 1: Differential Termination ONLY

With an external load connected, the output CM current splits between the internal TERM pin and the external load. However, with the configuration shown in Figure 7 and simplified in Figure 8, with no external CM DC current path to ground, the entire output CM current must flow through the internal TERM resistor(s).

In Figure 8, the external loading by the ADC and the cable termination network of R1, and R2 has no effect on the CM loading of the LTC6563. The range of output CM voltage will be as follows:

$$V_{CMO} = I_O \bullet (50\Omega + 2R_{CM}) \quad (1)$$

For the ADJ setting of 00 where Io is 7mA (see Table 1 and Table 5) here is the computation of min V_{CMO} possible (corresponding to $R_{CM} = 2\Omega$):

$$V_{CMO}\ (\text{minimum}) = 7\text{mA} \bullet (50\Omega + 2 \bullet 2\Omega) = 380\text{mV} \quad (2)$$

At the other extreme of V_{CMO} when R_{CM} opens, the output CM voltage will only be limited to the LTC6563 output compliance voltage which is about 1V below V_{CC} (or about 2.3V with $V_{CC} = 3.3V$).

Naturally, if the ADJ setting is changed, the V_{CMO} range will vary accordingly. Table 5 shows the minimum computed output CM voltage, output full scale swing, and TIA gain (RT) for various ADJ settings applied to the circuit in Figure 7.

For a higher Transimpedance gain (RT) or higher ADC FS swing, higher ADJ output current settings can be chosen. Summary of how ADJ affects the TIA gain and differential output voltage swing is tabulated in Table 5.

Here is a sample calculation of the values in Table 5 (50Ω Net diff load, full tilt) for ADJ 00 as an illustration:

a. Output current values (ADJ 00) with max input current of 90µA (from Table 2): 12mA, 2mA

b. Net diff output load: 50Ω (25Ω on each output)

RT Calculation: $RT(k\Omega) =$

c. $$\frac{25\Omega[(12\text{mA} - 2\text{mA}) - (2\text{mA} - 12\text{mA})]}{90\mu\text{A}} = 5.56k\Omega$$

Table 5. CM Minimum Voltage and Other Operating Performance Values for Various ADJ Settings of Figure 7

ADJ1	ADJ0	CM/AVERAGE OUTPUT CURRENT I_O (mA)	RT (kΩ)	ADC FS DIFF VOLTAGE SWING WITH FULL TILT (mV_{P-P})	MIN CM VOLTAGE (mV)
0	0	7	5.6	500	380
0	1	14	11.1	1000	756
1	0	21	16.7	1500	1134
1	1	28	22.2	2000	1512

APPLICATIONS INFORMATION

d. ADC FS diff voltage calculation = 90µA • 5.56kΩ = 500mV$_{P-P}$

e. I_O CM/Average Output Current (from Table 1): 7mA

f. V_{CMO} (minimum) = I_O • (50Ω + 2 • 2Ω) = 380mV where I_O = 7mA, 50Ω is the TERM internal resistance, and the 2Ω is the internal R_{CM} minimum value

The data in Table 5 can be used to examine the real-world problem of driving the AD9094 ADC, the input requirements of which are shown below:

Differential Input Voltage Range: 1.44V$_{P-P}$ to 2.16V$_{P-P}$ (programmable)

Common Mode Voltage: 1.43V

As can be seen from Table 5, operating the LTC6563 with ADJ 10 falls in the range of the required AD9094 FS swing voltage (1.44V$_{P-P}$ to 2.16V$_{P-P}$), and also complies with the required AD9094 CM voltage (1.43V) by allowing an output CM voltage as low as 1.13V. Therefore, ADJ 10 is an appropriate setting for driving the AD9094.

Detailed Example 2: Lowering the CM Voltage with a Tee Resistor or External DC Termination to Ground

Adding a path to ground from the center of the load resistors (R1, and R2) can lower the CM voltage. This can be in the form of grounding the middle of R1, and R2, or alternatively adding a TEE resistor to ground to avoid dropping the CM voltage too low. This technique (shown in Figure 10) allows for more flexibility in aligning the TIA to an ADC or a given differential load and ADJ setting.

The TEE resistor will appear as double its value in the half-circuit. The equivalent CM load and CM voltage can be written as:

$$V_{CMO} = I_O \bullet [(50\Omega + 2R_{CM}) || (R1 + 2R_{TEE})] \quad (3)$$

Note that adding R_{TEE} to the schematic only affects the CM parameters of the circuit and has no bearing on the differential voltage swing and the resulting transimpedance gain of the circuit. A shunt capacitor to ground across R_{TEE} can be added to ensure no spurious AC signal appears at this node.

For the particular case of Figure 7 schematic modified to include R_{TEE} = 20Ω with ADJ = 11 (I_O = 28mA from Table 1), the AD9094 CM voltage requirement (1.43V) would be easily satisfied since the CM servo loop would be able to adjust the output CM from 1.1V minimum (with R_{CM} = 2Ω, previously 1.51V minimum from Table 5 without R_{TEE}) to >2.3V (device output compliance volage) maximum using Equation 3.

Operation without Internal CM Servo Loop

There may be applications where the CM servo loop function built into the LTC6563 is not needed, as would be the case if the TIA output is not used to drive an ADC.

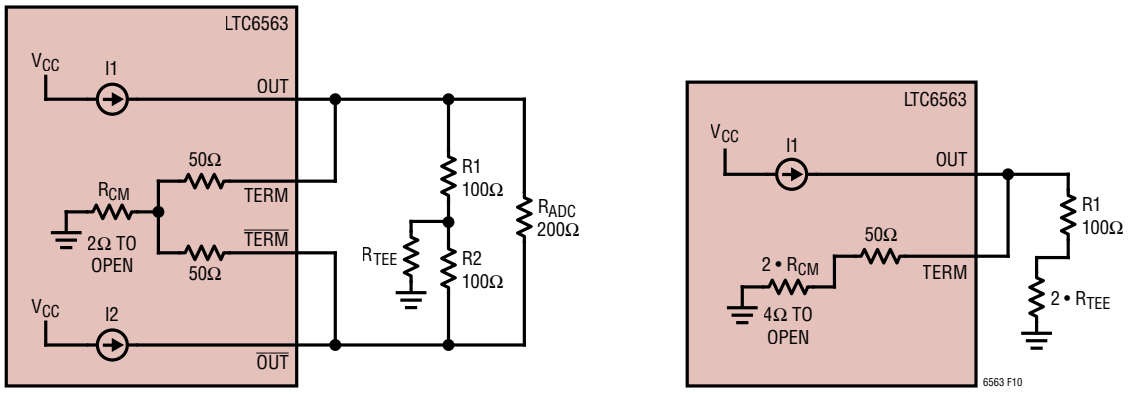


Figure 10. TEE Resistor Loading (Left) and Its Equivalent CM Half-Circuit (Right)

APPLICATIONS INFORMATION

Under these conditions, the following pin settings should be used:

1. TERM and $\overline{\text{TERM}}$ should be left floating.
2. An external circuit capable of sinking the output current must be used. This task is most easily accomplished by providing external termination to ground.
3. The CM pin *must* be tied to the expected output CM voltage. The output clamps levels are calculated from CM and HI pins, so failure to set the CM pin properly may result in undesired signal clamping.

When the TERM and $\overline{\text{TERM}}$ pins are left floating, the output CM voltage will be solely a function of the LTC6563 ADJ setting and the external CM load. For example, with ADJ11 setting (I_O = 28mA) and 50Ω to ground on each output, the output CM voltage will be:

$$V_{CMO} = I_O \bullet R_{LOAD\_CM} = 28mA \bullet 50\Omega = 1.4V \qquad (4)$$

With the CM servo loop function disabled, the LTC6563's CM pin should be tied to a voltage that is close to the expected CM value (1.4V in the example stated just above). The output clamp circuit assumes that CM is equal to the actual output CM voltage. If this is not the case, the clamping voltage set by the HI pin will be miscalculated, and undesired signal clipping may result. For this purpose, a replica V_{CMO} voltage can simply be generated off the device V_{CC} pin using kΩ range voltage division resistors.

Increasing Output Impedance

It may be desirable to change the output termination impedance in order to adjust the output signal amplitude. In addition, the flexibility of LTC6563's output structure allows for impedance matching to a variety of different loads or transmission line impedances, which is critical for high speed signal integrity. In the following example, the output circuit will be modified to present a 75Ω source impedance for driving a 75Ω transmission line and ADC load.

Consider the configuration shown in Figure 11 schematic. The output impedance of the LTC6563 is raised to 75Ω by adding 24.9Ω resistors in series with the internal 50Ω TERM resistors. The TIA now presents an output impedance that matches the 75Ω transmission line as well as the net ADC-side SE impedance. The transmission line ADC-side impedance can be calculated by:

((200Ω/2) + (2 • 4.99) || 300 Ω) = 80Ω.

Let's now take a look at the output CM voltage that pertains to the schematic of Figure 11, simplified in Figure 12:

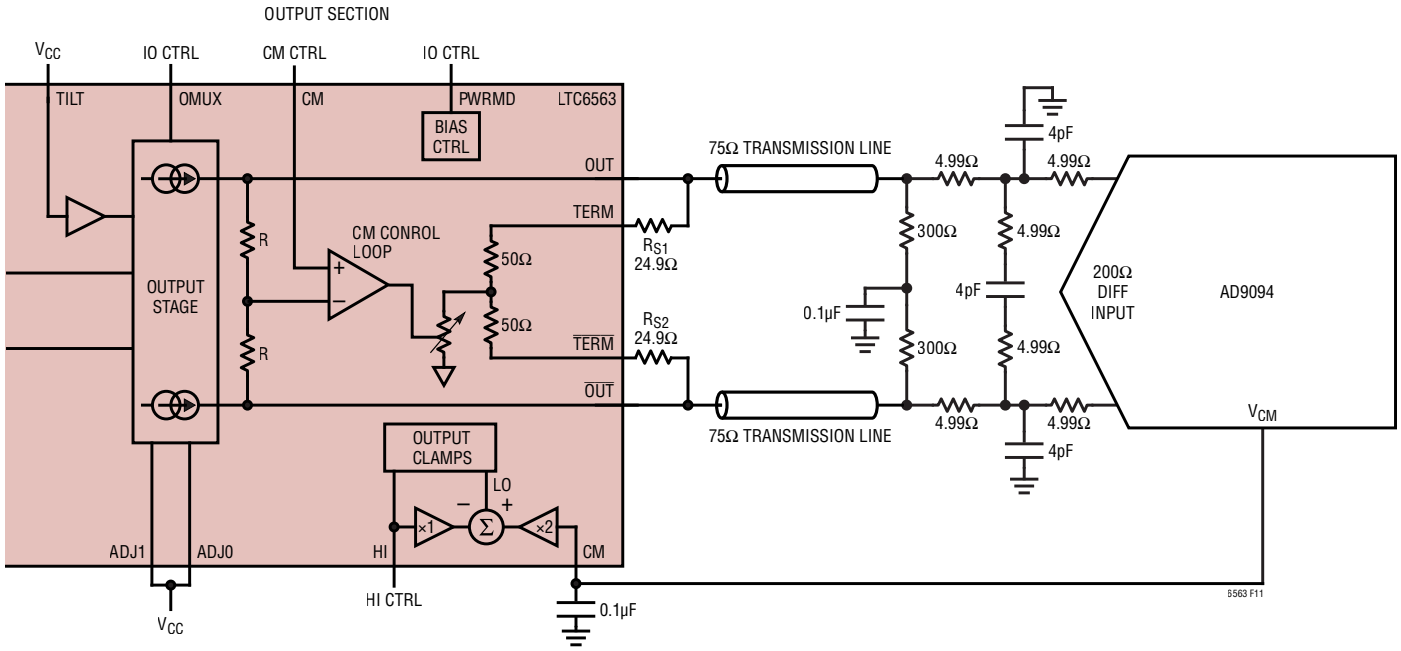


Figure 11. Increasing Diff Load Resistance and Matching to 75Ω

APPLICATIONS INFORMATION

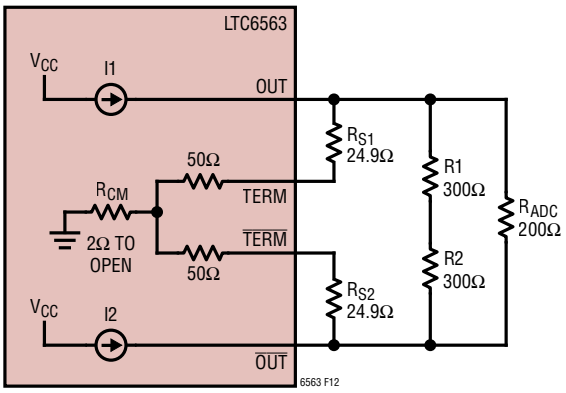


Figure 12. TIA 75Ω Matched Load Equivalent Circuit

As in the previous cases, for analysis purposes, it is useful to break the output load circuit into its equivalent half-circuit to compute how the CM voltage is affected, as shown in Figure 13.

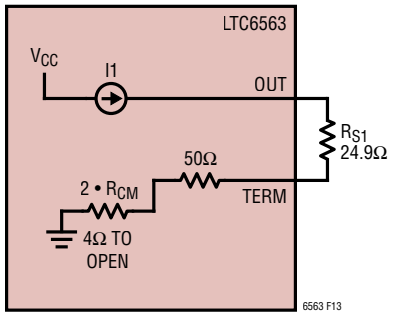


Figure 13. CM Half-Circuit Equivalent Circuit for 75Ω Load

As before, the CM circuit is not affected by the R1, R2 or the ADC differential input impedance of 200Ω. The output CM will be given by:

$$V_{CMO} = I_O \bullet (24.9\Omega + 50\Omega + 2R_{CM}) \qquad (5)$$

So, in addition to raising the TIA output impedance, R_{S1} and R_{S2} also contribute to an increase in the minimum output CM voltage.

Table 6 shows the computed minimum CM voltage, TIA gain (RT), and ADC FS diff voltage swing for various ADJ settings applied to the Figure 11 configuration.

Here is a sample calculation of the values in Table 6, related to the Figure 11 schematic, for ADJ 00 as an illustration:

a. Output current values (ADJ 00) with max input current of 90µA (from Table 2): 12mA, 2mA

b. Net diff output load: 75Ω (37.5Ω on each output)

RT Calculation: RT(kΩ) =

c. $$\frac{37.5\Omega[(12mA - 2mA) - (2mA - 12mA)]}{90\mu A} = 8.3k\Omega$$

d. ADC FS diff voltage calculation = 90µA • 8.3kΩ = $750mV_{P-P}$

e. I_O CM / Average Output Current (from Table 1): 7mA

f. V_{CMO} (minimum) = I_O • (24.9Ω + 50Ω + 2 • 2Ω) = 553mV, where I_O = 7mA, 24.9Ω is the resistors in series with the TERM pin, 50Ω is the TERM internal resistance, and the 2Ω is the internal R_{CM} minimum value

In the Figure 11 schematic and tabulated results in Table 6, the ADJ 11 setting's Min CM voltage is too high to be usable. Thus, the technique of lowering CM voltage (Detailed Example 2) discussed earlier can be employed

Table 6. CM Minimum Voltage and Other Operating Performance Values for Various ADJ Settings of Figure 11

ADJ1	ADJ0	CM/AVERAGE OUTPUT CURRENT I_O (mA)	RT (kΩ)	ADC FS DIFF VOLTAGE SWING WITH FULL TILT (mV_{P-P})	MIN CM VOLTAGE (mV)
0	0	7	8.3	750	553
0	1	14	16.7	1500	1106
1	0	21	25.0	2250*	1659
1	1	28	33.3	3000*	2212*

*Limited by output voltage compliance

APPLICATIONS INFORMATION

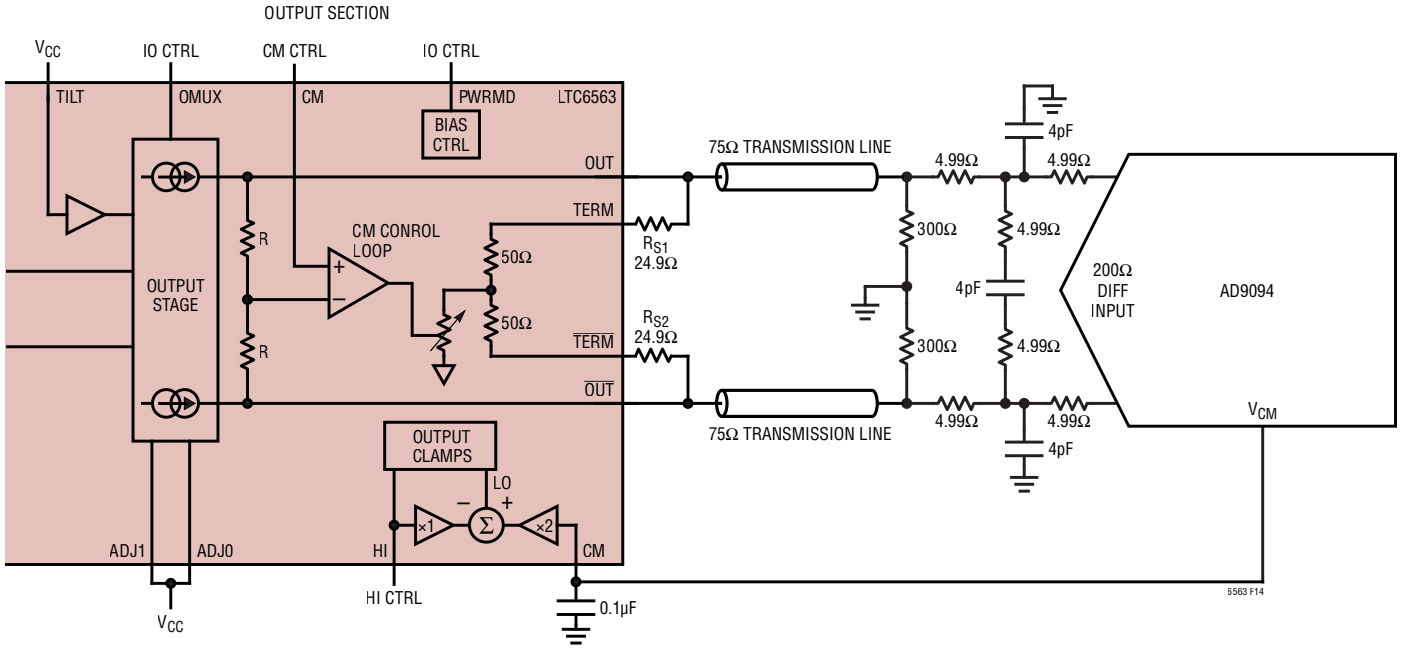


Figure 14. Reducing the Min CM Voltage with Grounding the External Load Midpoint

if ADJ 11 is to be used as shown in Figure 14 where the external loads (300Ω) mid-point is grounded.

With the modified schematic of Figure 14 the CM voltage is:

$$V_{CMO} = I_O \bullet [(24.9\Omega + 50\Omega + 2R_{CM})||300\Omega] \quad (6)$$

Resulting in the min VCMO for ADJ 11:

V_{CMO} (minimum) = $I_O \bullet [(24.9\Omega + 50\Omega + 2 \bullet 2\Omega)||300\Omega]$ = 28mA • 62.5Ω = 1.75V (7)

Table 7 shows the computed minimum CM voltage, TIA gain (RT), and ADC FS diff voltage swing for various ADJ settings applied to the Figure 14 configuration:

Here is a sample calculation of the values in Table 7, related to the Figure 14 schematic, for ADJ 00 as an illustration:

a. Output current values (ADJ 00) with max input current of 90µA (from Table 2): 12mA, 2mA

b. Net diff output load: 75Ω (37.5Ω on each output)

RT Calculation: RT(kΩ) =

c. $$\frac{37.5\Omega[(12mA - 2mA) - (2mA - 12mA)]}{90\mu A} = 8.3k\Omega$$

d. ADC FS diff voltage calculation = 90µA • 8.3kΩ = 750mV_{P-P}

Table 7. CM Minimum Voltage and Other Operating Performance Values for Various ADJ Settings of Figure 14

ADJ1	ADJ0	CM/AVERAGE OUTPUT CURRENT I_O (mA)	RT (kΩ)	ADC FS DIFF VOLTAGE SWING WITH FULL TILT (mV_{P-P})	MIN CM VOLTAGE (mV)
0	0	7	8.3	750	437
0	1	14	16.7	1500	875
1	0	21	25.0	2250*	1312
1	1	28	33.3	3000*	1750

*Limited by output voltage compliance

APPLICATIONS INFORMATION

e. I_O CM/Average Output Current (from Table 1): 7mA

f. V_{CMO} (minimum) = I_O • [(24.9Ω + 50Ω + 2 • 2Ω)||300Ω] = I_O • [78.9Ω||300Ω] = I_O • 62.5Ω = 437mV, where I_O = 7mA, 24.9Ω is the resistors in series with the TERM pin, 50Ω is the TERM internal resistance, and the 2Ω is the internal R_{CM} minimum value.

As can be seen, the only difference between Table 6 and Table 7 is in the last column, Min CM voltage, where this column's values are lowered in Table 7 by grounding the mid-point of the external load resistors.

Summary of TIA Operating Conditions and Their Effects

The current output nature of the LTC6563 provides a great deal of flexibility in tailoring the circuit to drive a variety of ADCs, transmission lines, or other loads that are found in various applications. The TIA gain (RT), full scale swing (FS), and output CM voltage design can be optimized using internal termination networks, external termination networks (ground referenced and differential), and ADJ settings.

Designing the TIA load and operational settings involves juggling these interdependent parameters. See Table 8 for a summary of how different TIA output operating conditions influence various important aspects of the TIA design:

Clamp Function

LTC6563 has internal output voltage clamps that restrain its differential output swing. These clamps maintain control of the OUT and $\overline{OUT}$ voltages to prevent overloading the ADCs inputs. The clamping speed is on the order of the TIA bandwidth so the ADCs functionality and signal integrity will be minimally affected by output signals that would otherwise exceed the ADCs input range.

OUT and $\overline{OUT}$ will be confined to the range of voltages shown below:

Maximum output high side voltage = HI pin voltage

Minimum output low side voltage = V_{CM} – (HI – V_{CM}) = $2V_{CM}$ – HI

Please remember that V_{CM} is the pin voltage of the CM input. If the actual output CM voltage differs from the CM pin voltage, unexpected clamping may occur.

Consider the example where, with CM = 1.4V and HI = 2.2V. The difference between CM and HI is 0.8V, so the outputs will be clamped between 1.4V ±0.8V. The OUT pin will not exceed 2.2V due to an input signal. At the same time, $\overline{OUT}$ will be limited to the same swing below the CM voltage or 1.4V – 0.8V = 0.6V. Done this way, a symmetrical swing is guaranteed whilst a single input voltage dictates the voltage limit in both swing directions.

It is critical that the voltage applied to the CM device pin represents the actual output CM voltage, otherwise the clamp(s) will not function correctly. With the TERM pins utilized, this requires a valid servo operation where LTC6563 maintains the output CM voltage. When the CM servo loop is not utilized (i.e. TERM and $\overline{TERM}$ are open), the clamps can still function as long as the CM pin is tied to a voltage that is close to the actual output CM voltage.

Table 8. Summary of LTC6563 Output Operating Conditions and Their Performance Effect

OPERATING CONDITION	EFFECT ON OUTPUT CM	EFFECT ON OUTPUT FS SWING	EFFECT ON TOTAL POWER DISSIPATION	EFFECT ON OVERALL GAIN	EFFECT ON SOURCE IMPEDANCE WHEN DRIVING TRANSMISSION LINE
R_{LDIFF} Value Increase	No Effect	Increase	No Effect	Increase	Increase
Add/Increase R in Series with TERM	Increase	Increase	No Effect	Increase	Increase
R_{TEE} Value Decrease	Reduce	No Effect	No Effect	No Effect	No Effect
ADJ (Logic Input) Increase	Increase	Increase	Increase	Increase	No Effect

APPLICATIONS INFORMATION

Avoiding Zero-Input Signal Clipping when Using TILT along with Clamp

Clamp operation is meant to mainly safeguard against transient overload conditions. Under normal operation, ensure that the clamps are not engaged with nominal signal levels and/or zero input current signal! To do this, set the HI input above the expected output voltage, or alternatively, tie HI input to V_{CCI} to disable clamp operation. When the TILT input is used to maximize the output swing, the voltage applied to the TILT input should be just enough to provide the required differential full-scale voltage without running the output(s) to the clamp region.

Referring to Figure 15 for this particular operating point example:

- ADJ =11, R_L = 50Ω to ground on each output pin, V_{CM} pin tied to 1.5V to match actual output CM voltage since CM servo loop is not used here

If clamps are used, set TILT to 1.3V, which is just above the Tilt voltage needed to ensure the maximum output swing can be achieved without running into the clamp(s). In this example, the HI pin should be tied to approximately 2V or higher. If clamps are disabled (HI pin tied to V_{CCI}), TILT input can simply be tied to V_{CCI} since running into the clamps is not an issue.

Output Tilt Control

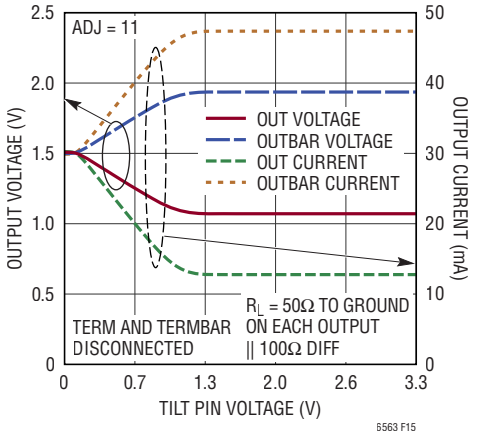
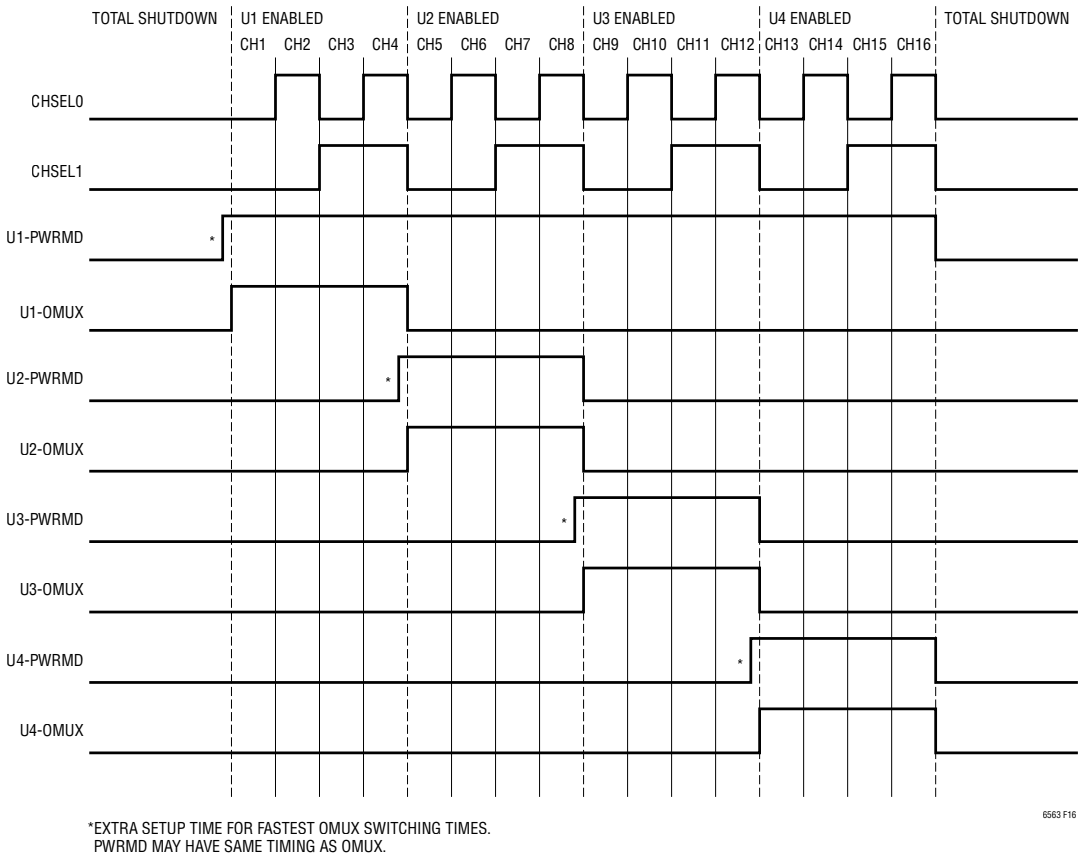


Figure 15. Tilt Input Transfer Function Example (ADJ11) with no TIA Input Current

Limitations of Output Clamp Architecture

The out clamps will only prevent overload scenarios that originate from the LTC6563's signal chain itself. Overloads caused by external stimuli at the LTC6563's may not be clamped, e.g. injecting current into the LTC6563's output(s).

TYPICAL APPLICATIONS



*EXTRA SETUP TIME FOR FASTEST OMUX SWITCHING TIMES.
PWRMD MAY HAVE SAME TIMING AS OMUX.

Figure 16. Timing Diagram for OMUX and Channel Control

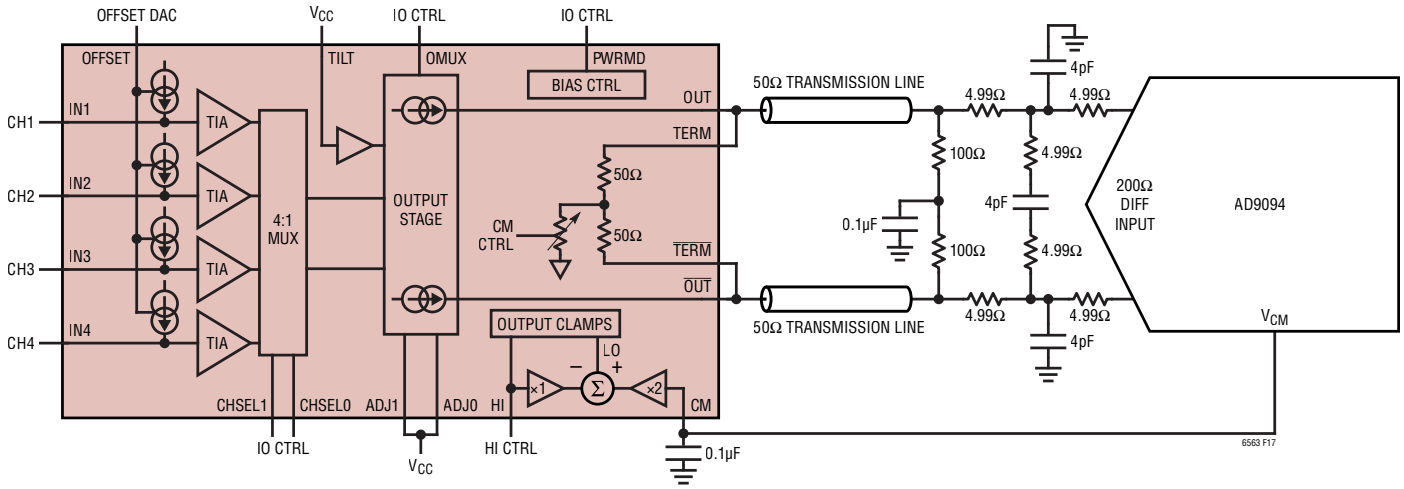


Figure 17. LTC6563 50Ω Transmission Line Circuit

TYPICAL APPLICATIONS

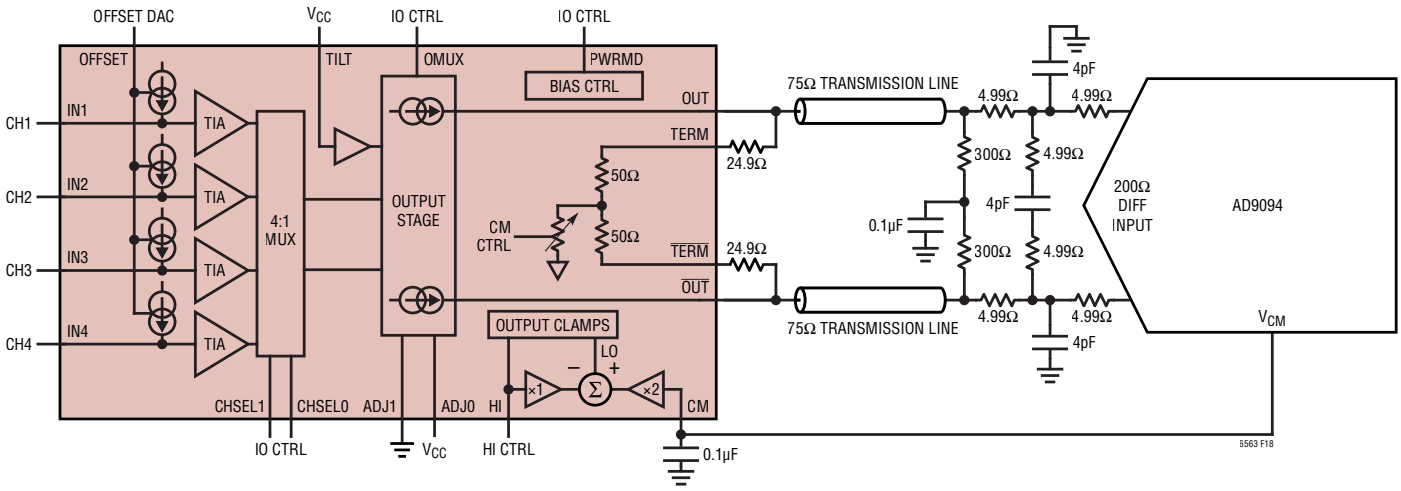


Figure 18. LTC6563 75Ω Transmission Line Circuit

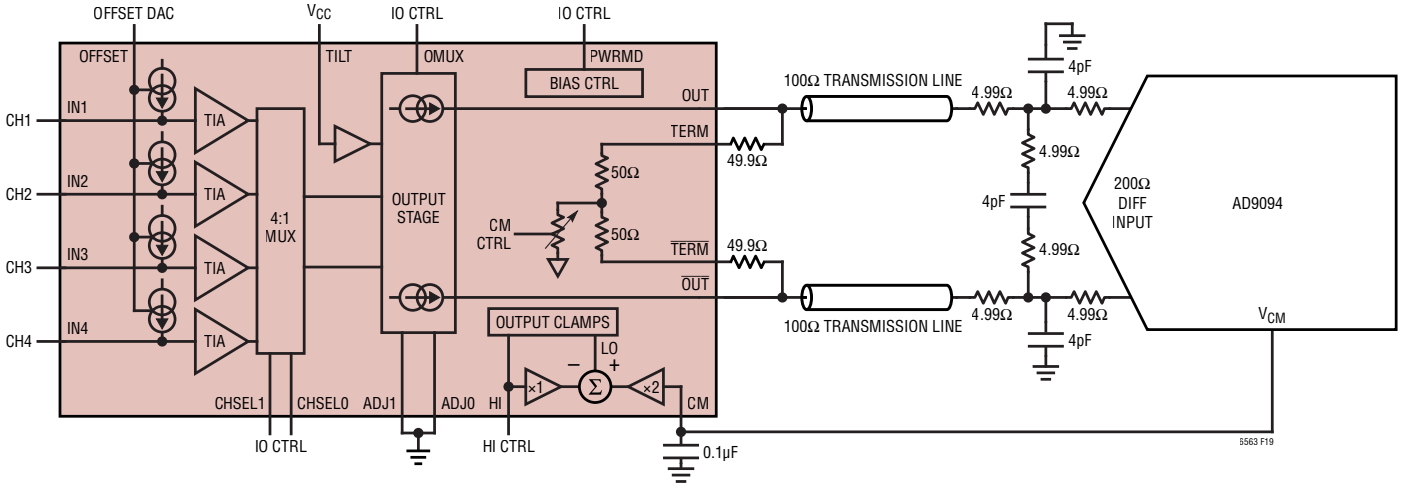
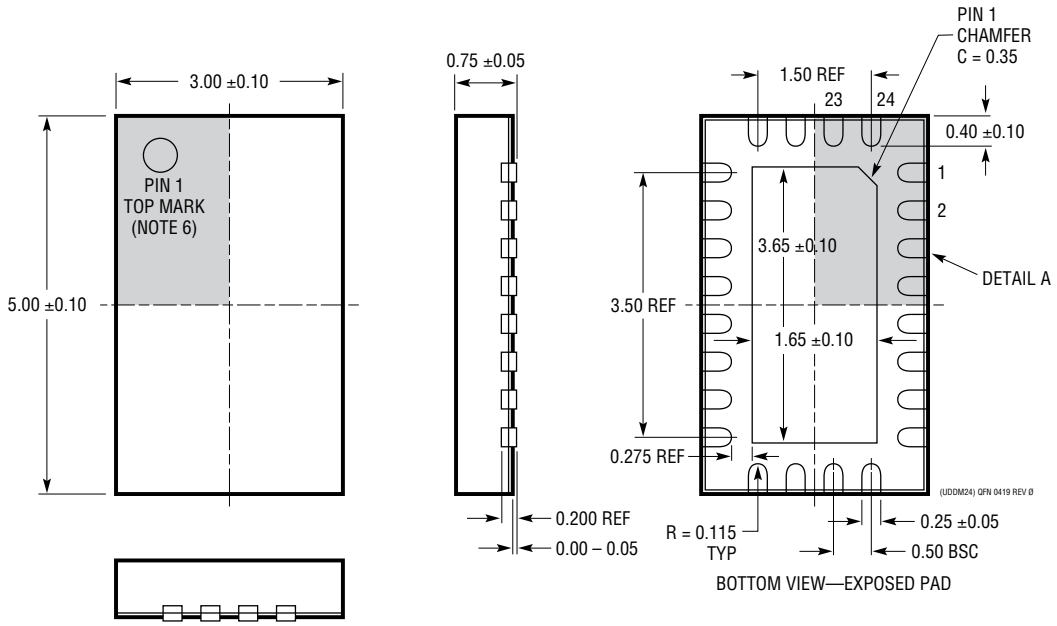
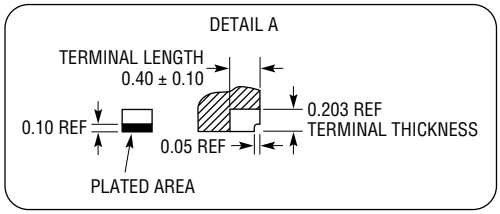


Figure 19. LTC6563 100Ω Transmission Line Circuit

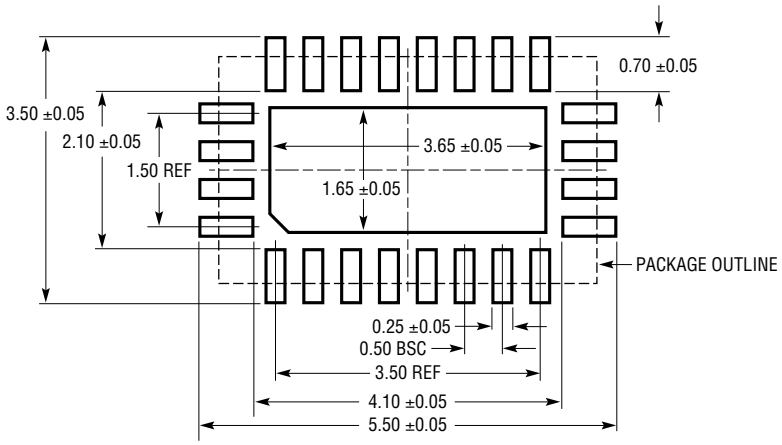
PACKAGE DESCRIPTION

UDDM Package
24-Lead Plastic Side Solderable QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1795 Rev Ø)





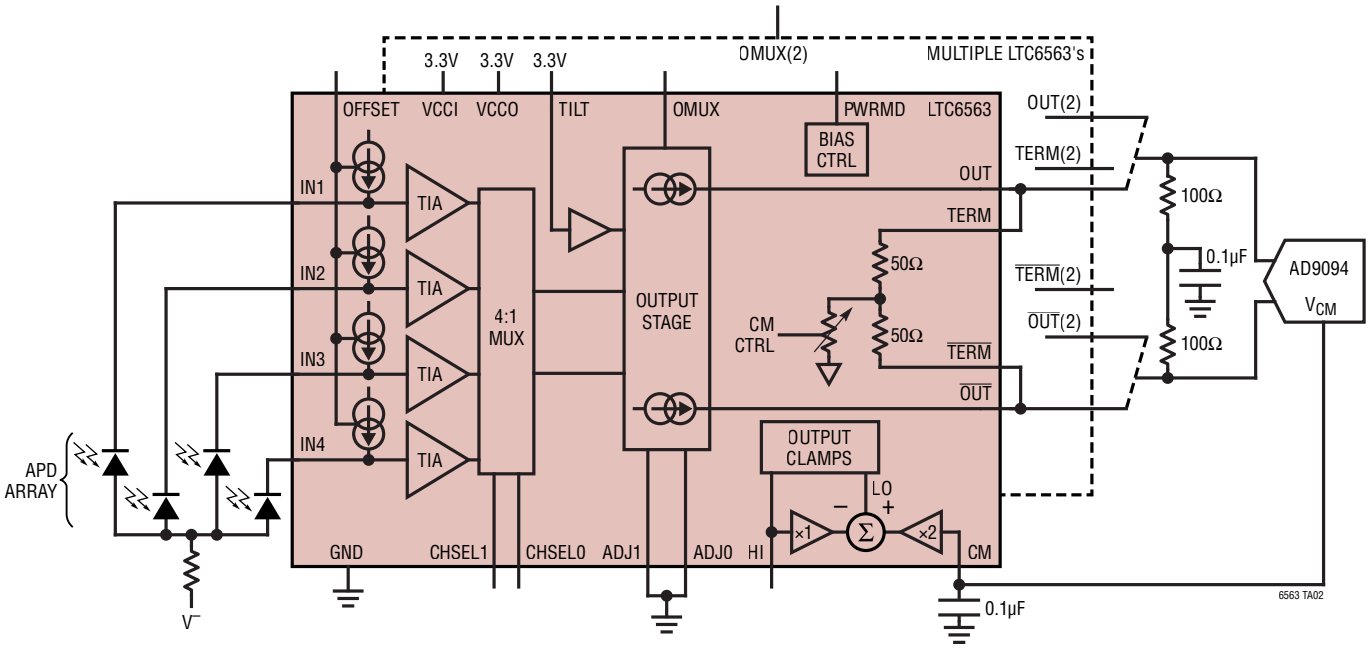
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

TYPICAL APPLICATION

Typical Application with DC-Coupled Inputs Driving an ADC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6560	1-Channel Transimpedance Amp with Output Muxing	220MHz, 74kΩ Transimpedance S/E Output
LTC6561	4-Channel Transimpedance Amp with Output Muxing	220MHz, 74kΩ Transimpedance S/E Output
AD8465	Single-Supply LVDS Comparator	1.6ns Propagation Delay
ADCMP604	Single-Supply LVDS Comparator	1.6ns Propagation Delay
LTC6754	High Speed Rail-to-Rail Input Comparator with LVDS Compatible Outputs	1.8ns Propagation Delay
LTC6752	280MHz Comparator	2.9ns Propagation Delay
LTC6268	500MHz Ultra Low Bias Current FET Input Op Amp	GBW = 500MHz, –3dB BW = 350MHz, I_b = ±3FA
LTC6268-10	4GHz Ultra Low Bias Current FET Input Op Amp	De-Comped Version of the LTC6268, GBW = 4GHz
LTC6409	10GHz Bandwidth, 1.1nV/√Hz Differential Amplifier/ADC Driver	GBW = 10GHz, e_n = 1.1nV/√Hz
AD9094	8-Bit, 1 GSPS, JESD204B, Quad Analog-to-Digital Converter	4x JESD204B
AD9694	Quad 14-Bit, 500Msps, 1.2V/2.5V ADC	4x JESD204B
LT8331	Low I_Q Boost/SEPIC/Flyback/Inverting Converter	0.5A, 140V Switch
LT8365	Low I_Q Boost/SEPIC/Inverting Converter	1.5A, 150V Switch