RAA211230

24V 3A Integrated Switching Regulator

The RAA211230 is an integrated 24V, 3A synchronous buck regulator with Constant On-Time (COT) current mode control. The RAA211230 features comprehensive protection including Input Undervoltage Lockout (UVLO), Overcurrent Protection (OCP), Output Undervoltage Protection (OUVP), and Over-Temperature Protection (OTP).

The device is available in a 6 Ld TSOT23 package.

Applications

- General purpose
- Industrial power supplies
- Embedded systems and I/O supplies

Features

- 4.5V to 24V input supply range
- Integrated high-side (100mΩ) and low-side (50mΩ) MOSFETs
- 500µA quiescent current
- Variable load dependent switching frequency with minimum on-time of 70ns typical and minimum off-time of 250ns typical
- 0.768V reference voltage with 2% accuracy (room temperature)
- PFM mode under light load condition
- Current mode Constant On-Time (COT) control with internal compensation
- Variable load dependent switching frequency
- Internal 1ms soft start time
- Protection: Low-Side Overcurrent (LSOC) limit, input Undervoltage Lockout (UVLO), Over-Temperature Protection (OTP), Output Undervoltage Protection (OUVP) with Hiccup Mode
- 6 LD TSOT23 package
- Output voltage programmable using a resistive divider on FB pin
- EN pin for sequence control

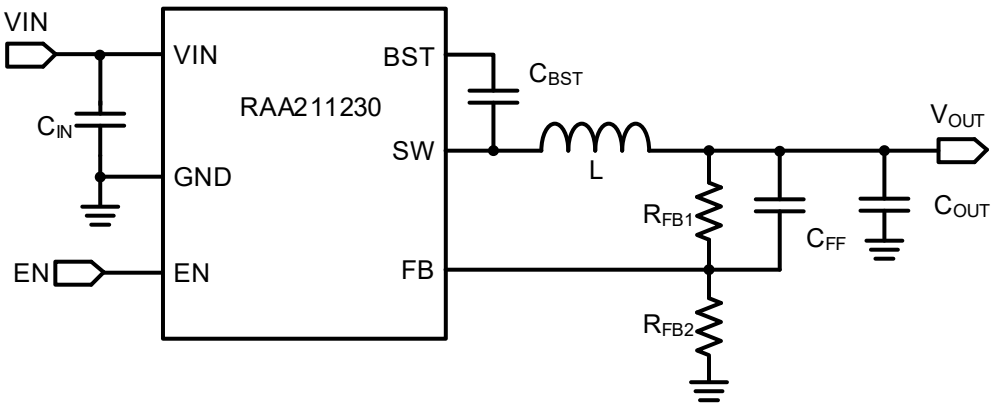


Figure 1. Typical Application Circuit Diagram

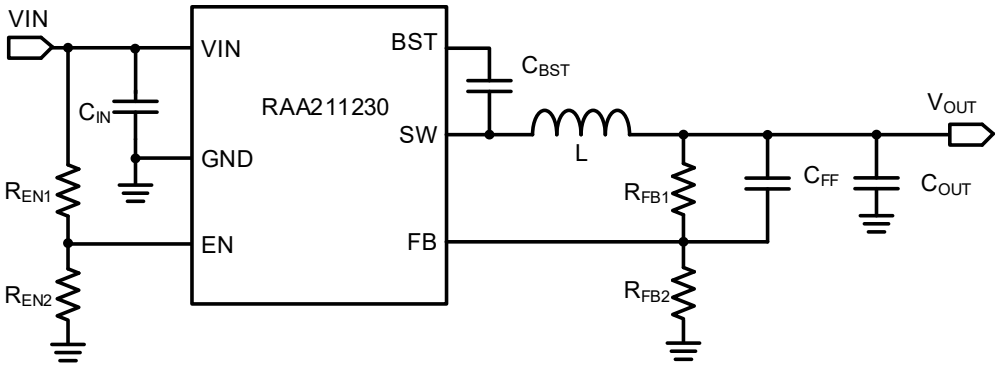


Figure 2. Typical Application Circuit Diagram with V_{IN} UVLO Programming by ENABLE

Table 1. Bill of Materials for Typical Application Circuit

Item	Qty	Reference	Value	Description	Part number
1	1	C_{IN}	10µF	CAP CER 10µF 35V X7R 1206	GMK316AB7106KL-TR
2	1	C_{OUT}	22µF	CAP CER 22µF 6.3V X7R 0805	GRM21BZ70J226ME44L
3	1	C_{BST}	0.1µF	CAP CER 0.1µF 10V X7R 0603	C0603C104K9RACTU
4	1	L_1	10µH	IHLP-2525CZ-ER-10-M-01	IND_IHLP-2525CZ-01
5	1	R_{FB1}	66k	1% resistor 0603	Generic
6	1	R_{FB2}	20k	1% resistor 0603	Generic

Contents

1. Overview

1.1 Block Diagram

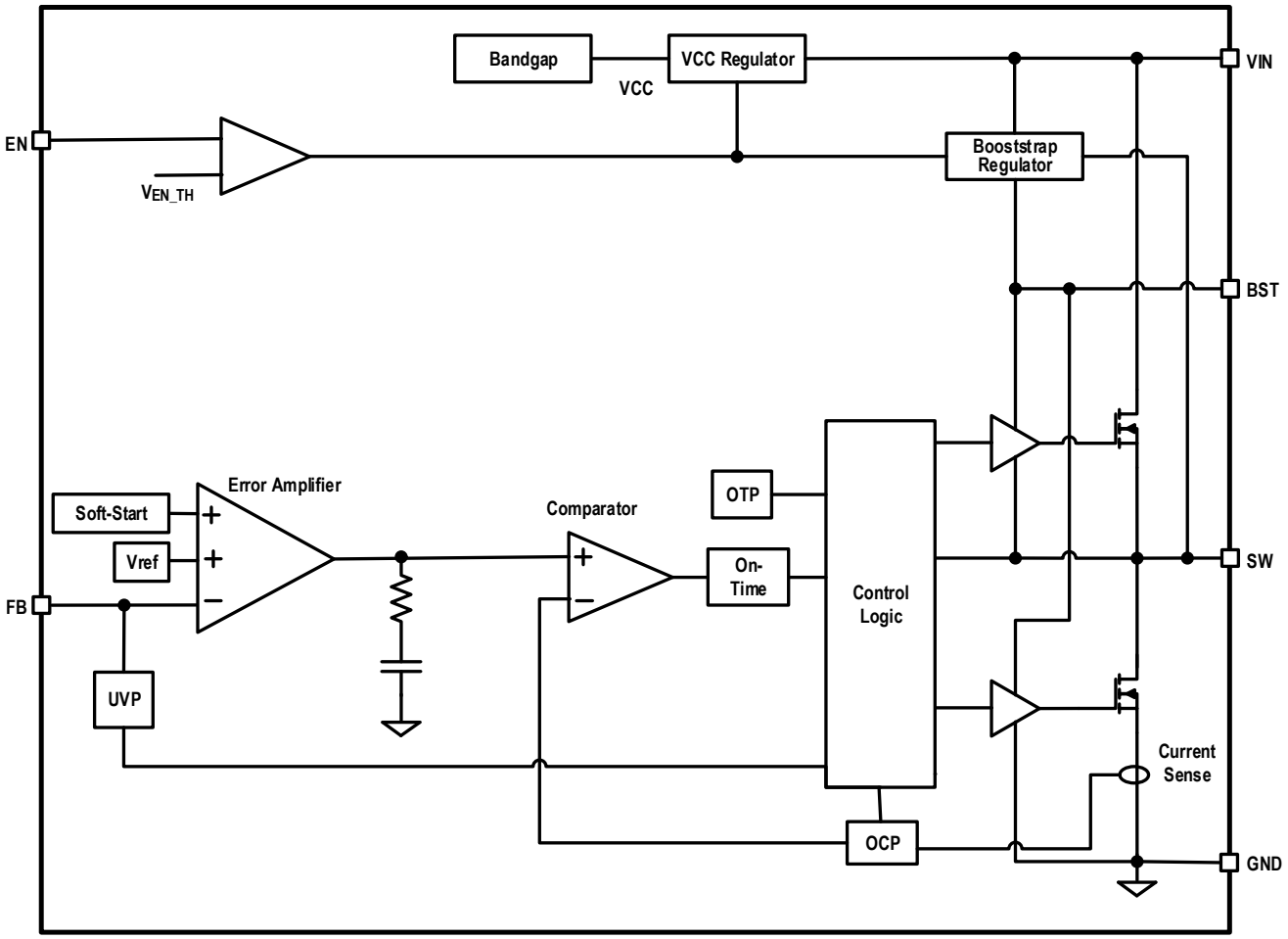
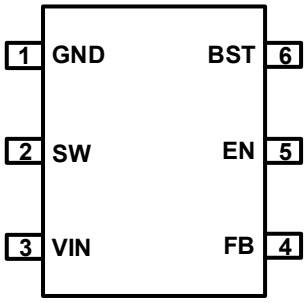


Figure 3. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	GND	Ground
2	SW	Switch node pin. Connect this pin to the output inductor and bootstrap capacitor.
3	VIN	Voltage input for the IC. Connect to a suitable voltage source within the IC operating range to this pin. Place a ceramic capacitor from VIN to GND close to the IC for decoupling.
4	FB	Feedback input pin for the regulator. The output voltage is set by an external resistor divider connected to FB. FB voltage is 0.768V ±2% across temperature range during normal operation.
5	EN	Accurate enable signal, accurate to ±5%.
6	BST	Bootstrap supply pin. Connect a 0.1µF capacitor from BST to SW.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN, EN	-0.3	26.5	V
SW	-0.7	V_{IN} + 0.3	V
BST		SW + 5.5	V
All other pins	-0.3	5	V
ESD Rating and Latch-Up	**Value**		**Unit**
Human body model (HBM) ESD stress voltage (Tested per JS-001-2017)	2		kV
Charged Device Model (CDM) ESD stress voltage (Tested per JS-002-2018)	0.75		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
6 Ld TSOT23	100 (TBD)	TBD

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-40	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Voltage, V_{IN}	4.5	24	V
Output Voltage, V_{OUT}	0.768	14	V
Output Current, I_{OUT}	0	3	A
Junction Temperature, T_J	-40	+125	°C

3.4 Electrical Specifications

$T_A = T_J$ = -40°C to +125°C, V_{IN} = 12V, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Symbol	Test Conditions	Minimum[1]	Typical	Maximum[1]	Unit
Supply Voltage						
V_{IN} Voltage Range	V_{IN}		4.5		24	V
Quiescent Current	I_Q	EN = 2V, VFB = 0.8V, no switching		500		µA
Shutdown Current	I_{SH}	EN = 0V, V_{IN} = 12, no switching		1	10	µA
V_{IN} Undervoltage Lockout		VIN Rising			4.45	V
V_{IN} Undervoltage Hysteresis		VIN Falling		360		mV
Output Voltage						
V_{OUT} Voltage Range	V_{OUT}	Determined by Minimum t_{OFF}	0.768		14	V
Enable Voltage						
EN Threshold Voltage	VEN	EN rising		1.29		V
Enable Voltage Hysteresis				0.1		V
Enable Shutdown Threshold	VENL			0.7		V
EN Pin Resistance to GND	REN	VEN = 2V		2000		kΩ
Switching Frequency and Timer Control						
Switching Frequency Range	f_{SW}	VFB = 0.768V, V_{OUT} = 1.05V, I_{OUT} = 1A, V_{IN} = 12V		500		kHz
Minimum Off-Time	t_{OFF_MIN}	VFB = 0.750V		250		ns
Minimum On-Time	t_{ON_MIN}	VFB = 0.780V		TBD		ns
Internal Soft-Start Time				1		ms
Feedback Voltage						
Feedback Voltage Reference	VFB	V_{IN} = 12V, EN = 2V, 25°C	0.753(-2%)	0.768	0.783(2%)	V
Feedback Voltage Line Regulation				±1		%/V
Internal Integrated MOSFETs						
High-Side On-Resistance	$r_{DS(ON)\_H}$	VBST-VSW = 4.8V(TBD)		TBD		mΩ
Low-Side On-Resistance	$r_{DS(ON)\_L}$			50		mΩ
Current Limit and Protection						
Current Limit	ILIM_L	Valley current, low-side FET, valid when t_{OFF} > 100ns	2.55	3	3.5	A
UVP	FB_UV	Fault threshold, VFB falling, soft-start completed		499		mV
Hiccup Soft-Start Done Time	t_{HICCUP_ON}			1.25		ms
Hiccup Power Off-Time	t_{HICCUP_OFF}			15		ms
Thermal Shutdown	TSD			170		°C
Thermal hysteresis	ΔTSD			20		°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

4. Faults and Fault Handling Description

4.1 System Level Fault Cases

Top level faults (VIN UVLO, OTP) disable VOUT and the IC enters the POR state until the fault is cleared. The device then resumes normal operation according to the state of the EN pin.

Fault Type	Detection Activated When	Detection Delay	Design Implementation
V_{IN} UVLO falling	EN is higher than threshold	2µs	POR, chip restarts from initial reset state when UVLO is satisfied.
Over-temperature (OT) shutdown	After EN pin goes high and IC is in active state.	immediate	POR using internal regulator, hiccup timer is engaged.
V_{OUT} Undervoltage (UV)	After soft-start done, after Hiccup on-time	immediate	VFB UV (65%) and LSOC after soft-start done, hiccup timer is engaged
Low-Side Overcurrent (LSOC) Limit	Start of buck regulator switching	immediate	If LSOC is detected, the device keeps LS FET on until current falls below LSOC limit.

5. Startup/Shutdown specification and application description

5.1 Case 1: EN=VIN with resistor

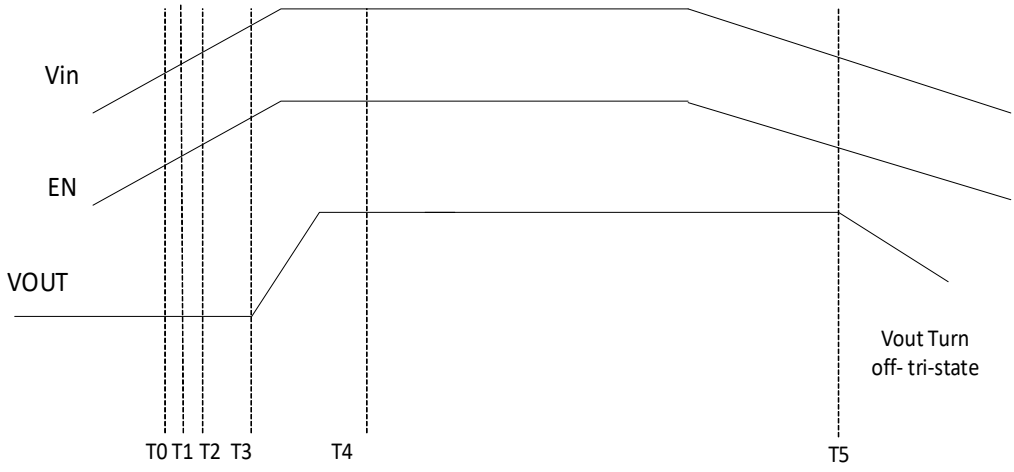


Figure 4.

EN = Vin

T0: EN low threshold=0.7V

T1: EN high threshold=1.5V

T2: VIN UVLO =4.45V max

T3: Vout soft start – ss time=2ms typical

T4: Vout soft start done

T5: Vin is less than UVLO falling edge, Vout shutdown

5.2 Case 2: EN=resistor divider from Vin, EN threshold causes device to be on/off

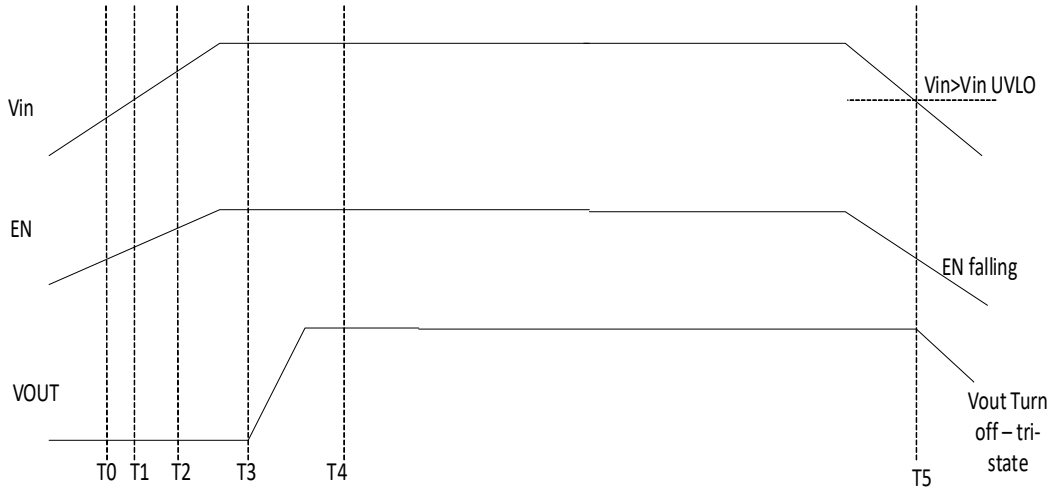


Figure 5.

EN = resistor divider from Vin

T0: VIN UVLO met, but no switching until EN threshold is reached

T1: EN low threshold=0.7V

T2: EN high threshold=1.29V

T3: Vout soft start

T4: Vout soft start done

T6: EN threshold detected, Vin> Vin UVLO, Vout shutdown due to EN falling below threshold

5.3 Case 3: EN = Logic signal>EN thresholds, prior to Vin application

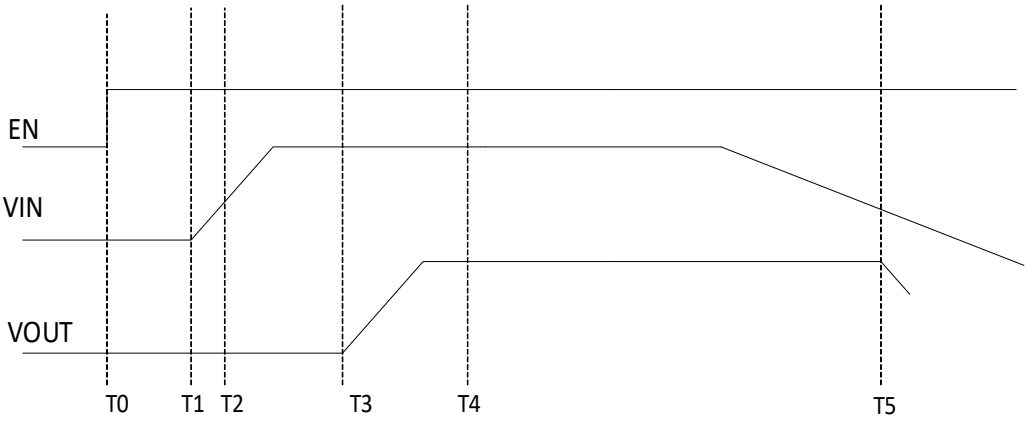


Figure 6.

EN = Logic signal>EN thresholds, prior to Vin application

T0: EN > 1.29V

T1: Vin ramp start

T2: Vin UVLO, device start due to Vin> UVLO threshold

T3: Vout Soft start

T4: Vout Soft start done

T5: VIN UVLO falling threshold trip, Vout shutdown due to Vin < UVLO threshold

5.4 Case 4: EN = Logic signal>EN thresholds, after Vin application

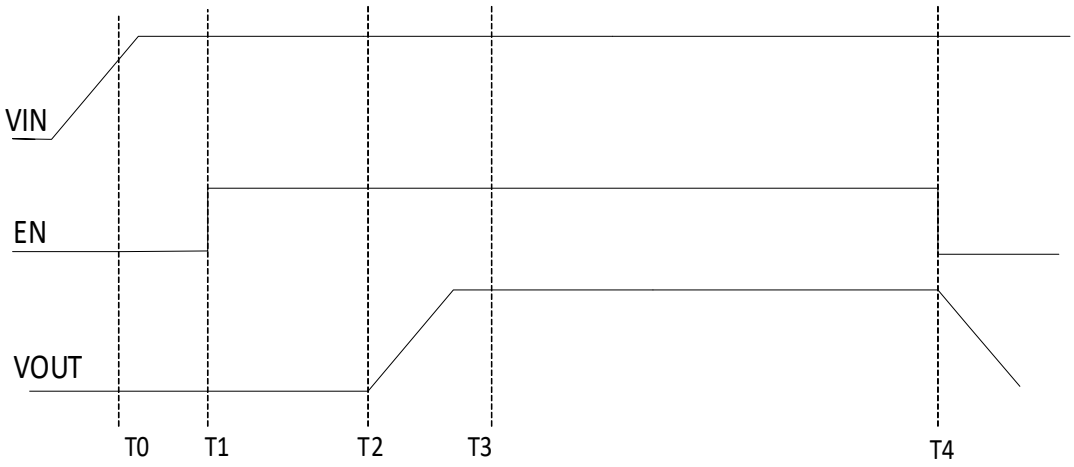


Figure 7.

EN = Logic signal<EN thresholds, prior to Vin application

T0: Vin UVLO threshold passed, but not being detected since EN is low

T1: EN> 1.29V

T2: Vout Soft start

T3: Vout Soft start done

T4: EN low threshold detected, Vin>Vin UVLO , Vout shutdown due to EN <threshold

6. Typical Performance Curves

Typical Values are at T_a = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, L = 3.3uH, unless otherwise noted

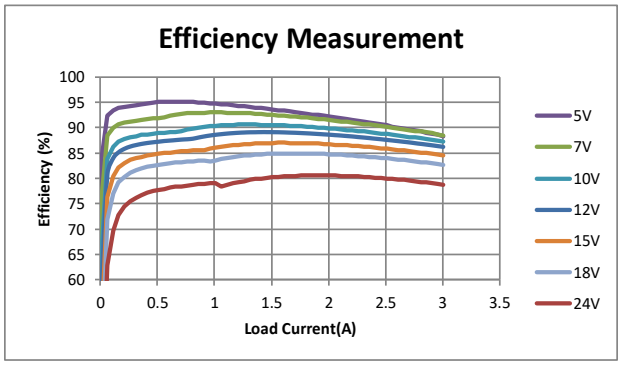


Figure 8. Efficiency vs Load Current (V_{OUT} = 3.3V)

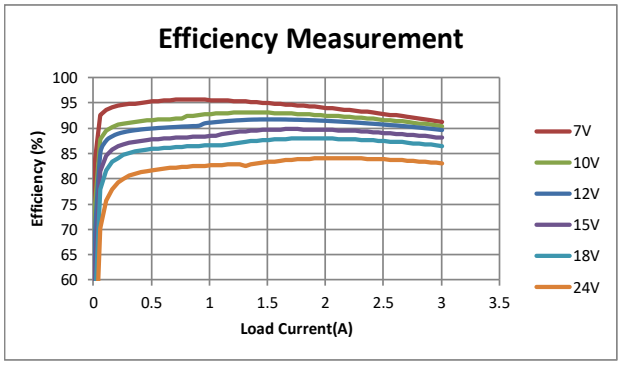


Figure 9. Efficiency vs Load Current (V_{OUT} = 5V)

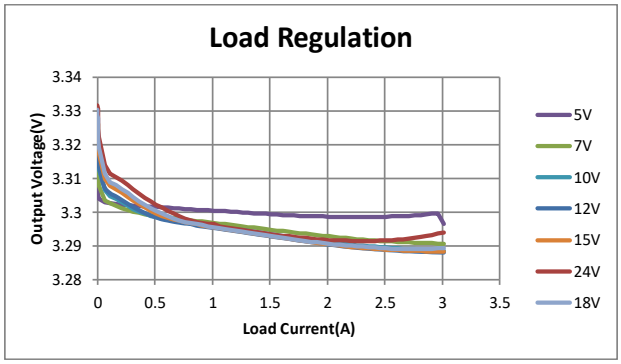


Figure 10. Load Regulation (V_{OUT} = 3.3V)

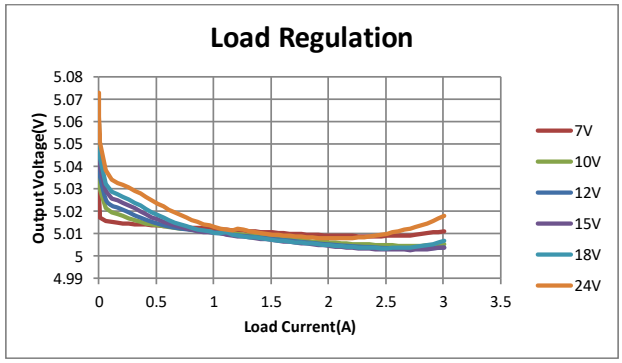


Figure 11. Load Regulation (V_{OUT} = 5V)

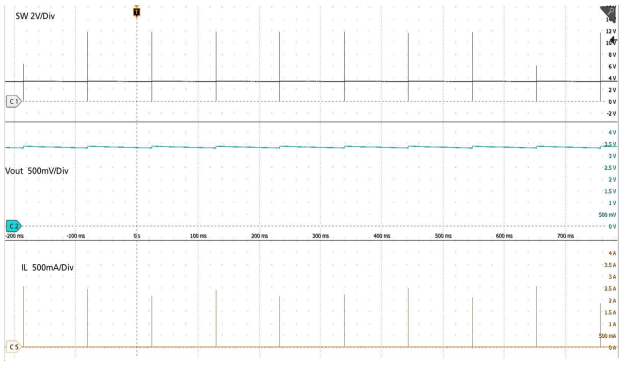


Figure 12. Steady-State Operation I_{OUT} = 0A (V_{OUT}=3.3V)

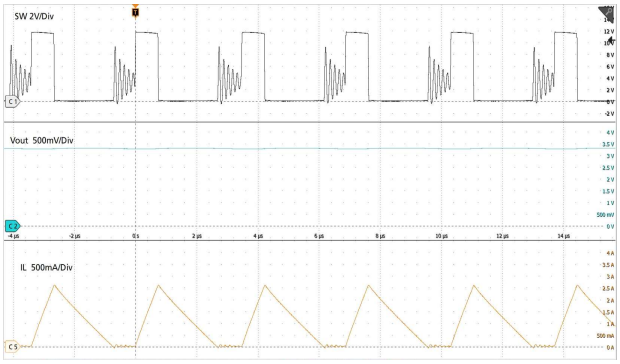


Figure 13. Steady-State Operation I_{OUT} = 1A(V_{OUT}=3.3V)

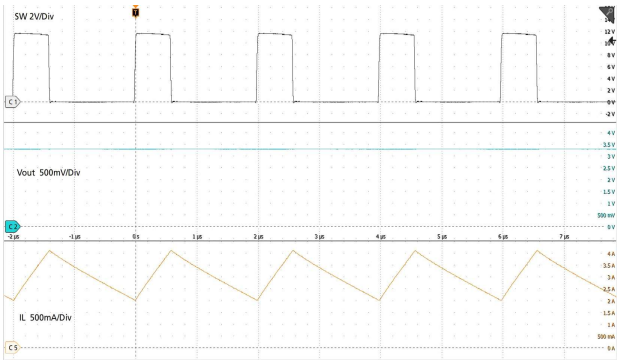


Figure 14. Steady-State Operation I_{OUT} = 3A (V_{OUT}=3.3V)

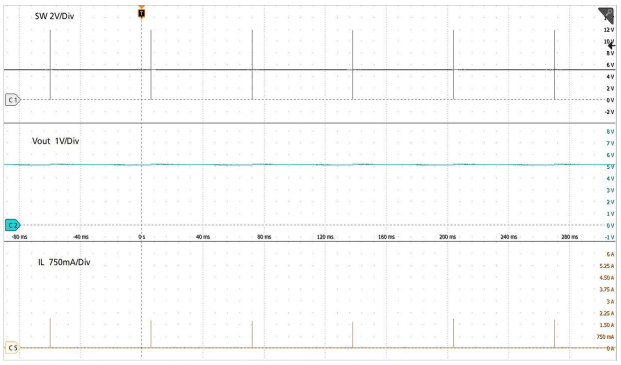


Figure 15. Steady-State Operation I_{OUT} = 0A(V_{OUT}=5V)

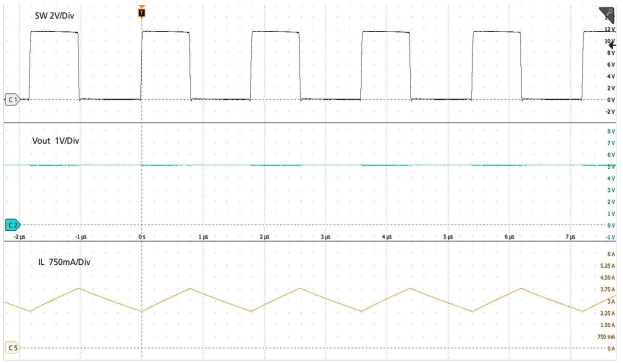


Figure 16. Steady-State Operation I_{OUT} = 3A (V_{OUT}=5V)

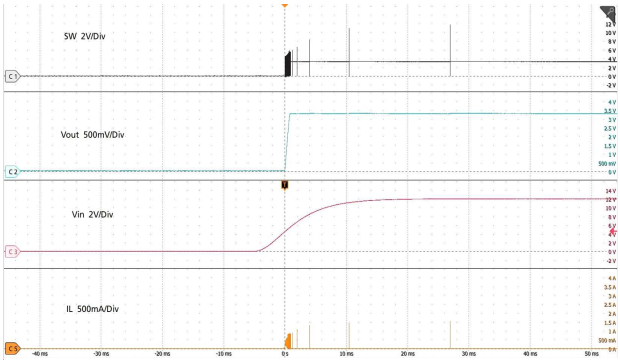


Figure 17. Startup through VIN (I_{OUT} = 0A)

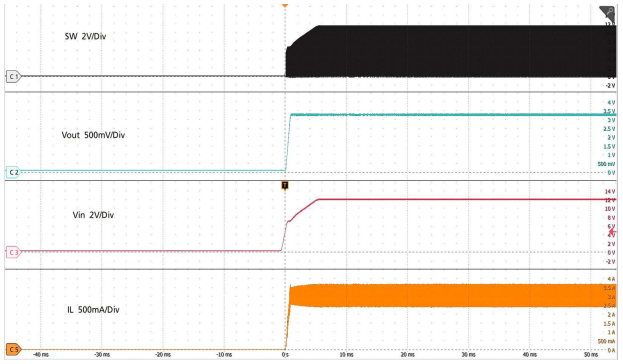


Figure 18. Startup through VIN (I_{OUT} = 3A)

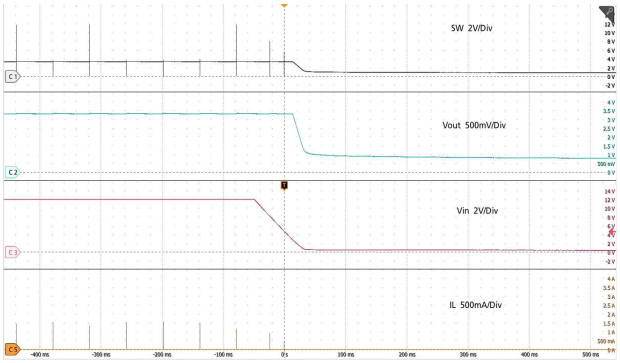


Figure 19. Shutdown through VIN (I_{OUT} = 0A)

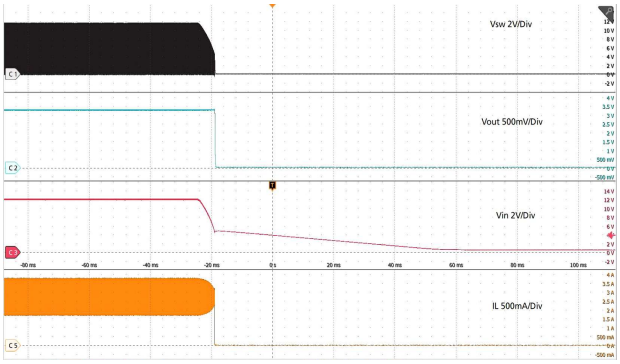


Figure 20. Shutdown through VIN (I_{OUT} = 3A)

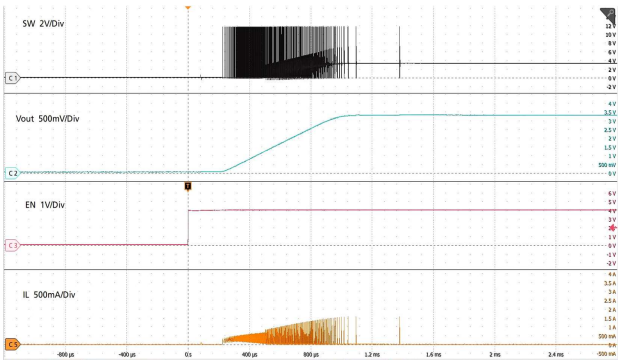


Figure 21. Startup through EN (I_{OUT} = 0A)

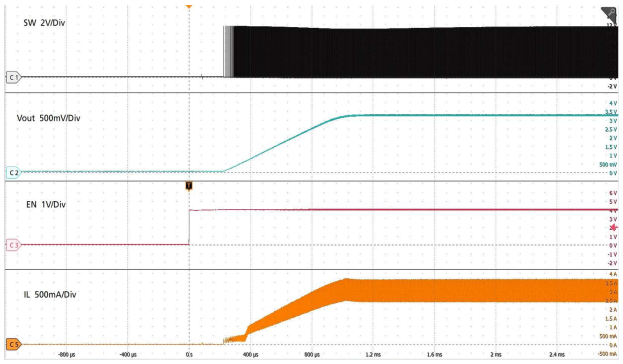


Figure 22. Startup through EN (I_{OUT} = 3A)

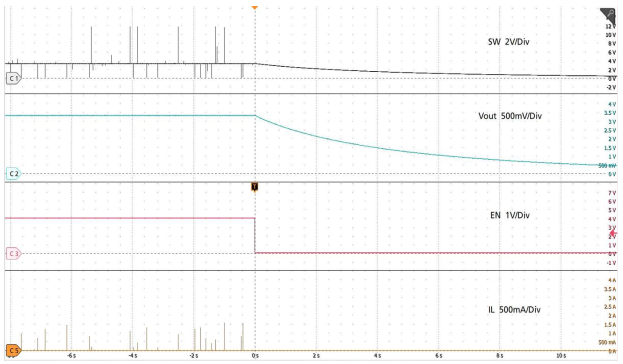


Figure 23. Shutdown through EN (I_{OUT} = 0A)

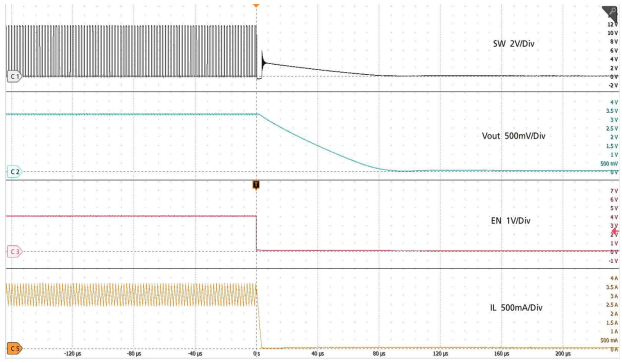


Figure 24. Shutdown through EN(I_{OUT} = 3A)

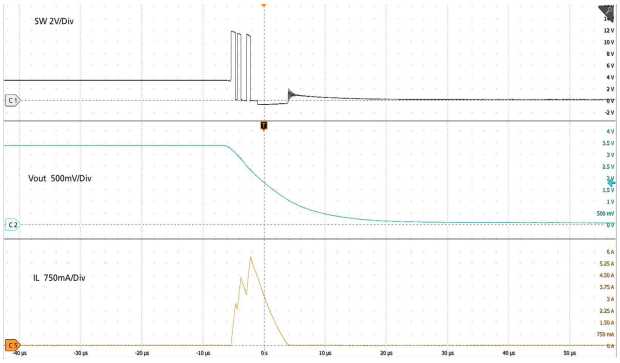


Figure 25. I_{OUT} = 0A to Short Circuit

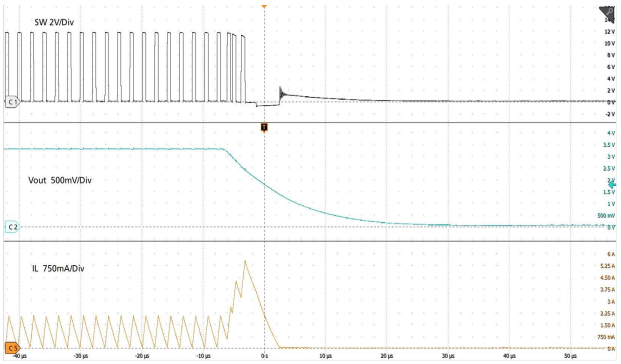


Figure 26. I_{OUT} = 1A to Short Circuit

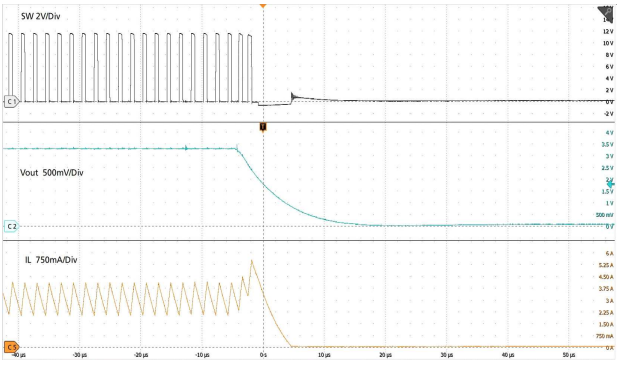


Figure 27. I_{OUT} = 3A to Short Circuit

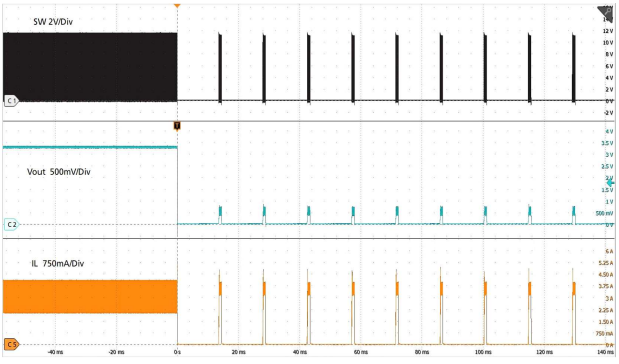


Figure 28. Hiccup after output Short Circuit

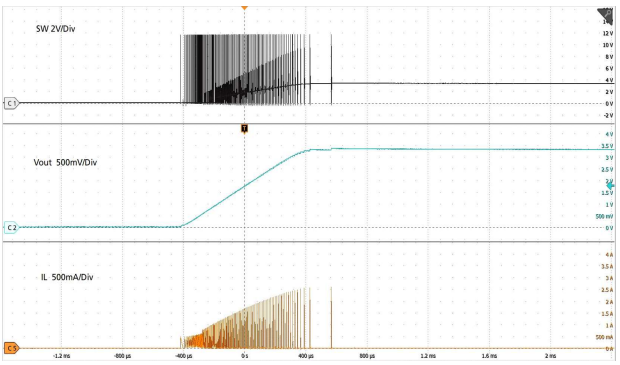


Figure 29. Short Circuit to 0A Recovery

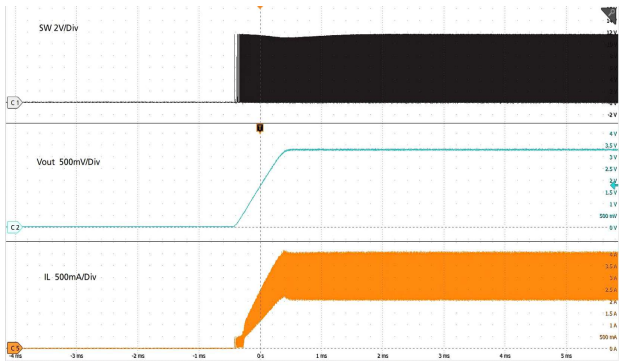


Figure 30. Short Circuit to 3A Recovery

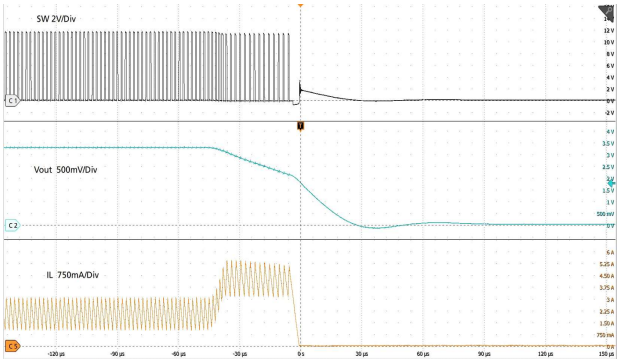


Figure 31. Low-Side Overcurrent (LSOC) Protection

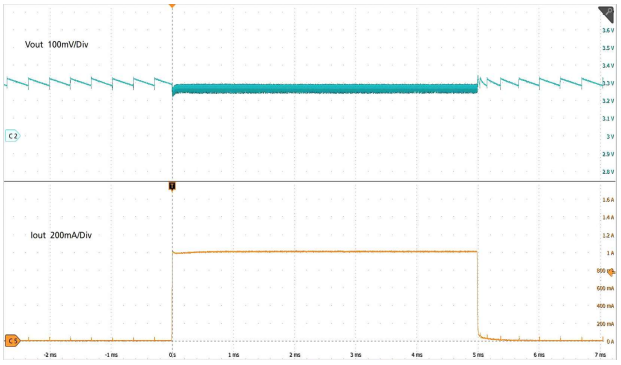


Figure 32. Load Transient IOUT = 0A -> 1A -> 0 (0.5A/µs)

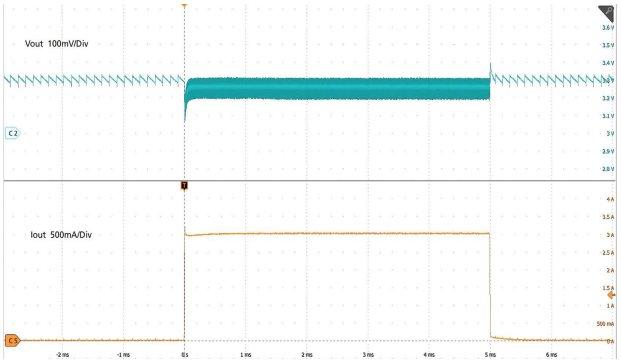


Figure 33. Load Transient IOUT = 0A -> 3A -> 0 (0.5A/µs)

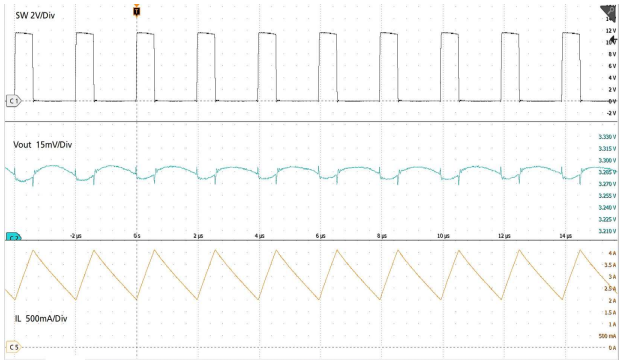


Figure 34. V_{OUT} Ripple at I_{OUT} = 3A (V_{OUT}=3.3V)

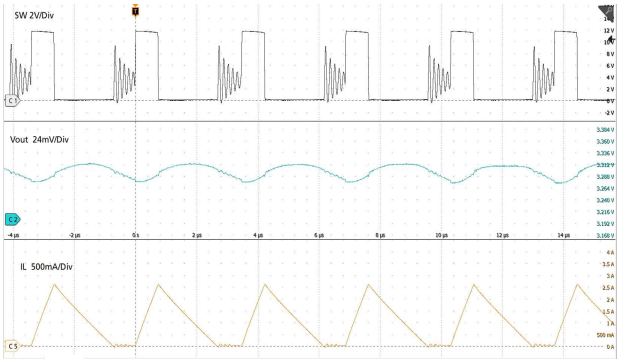


Figure 35. V_{OUT} Ripple at I_{OUT} = 1A (V_{OUT}=3.3V)

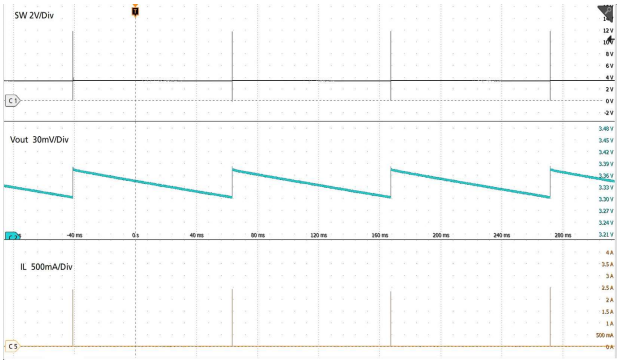


Figure 36. V_{OUT} Ripple at I_{OUT} = 0A (V_{OUT}=3.3V)

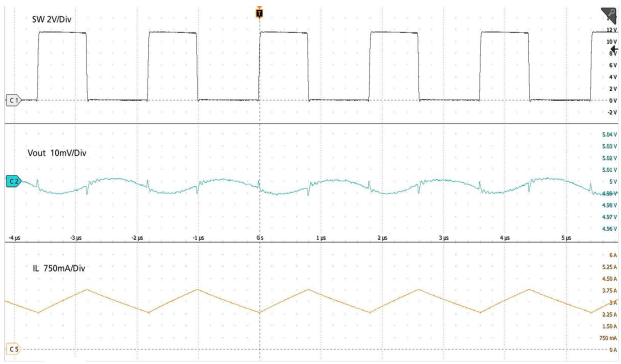


Figure 37. V_{OUT} Ripple at I_{OUT} = 3A (V_{OUT}=5V)

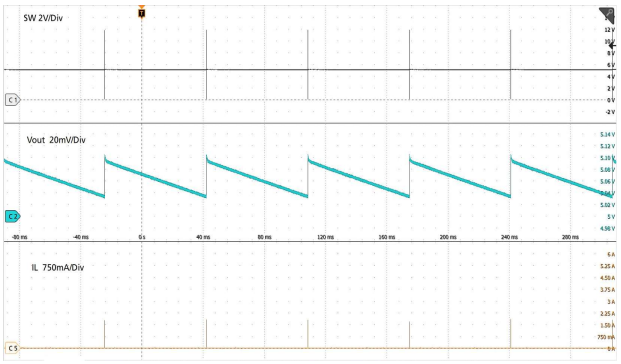


Figure 38. V_{OUT} Ripple at I_{OUT} = 0A (V_{OUT}=5V)

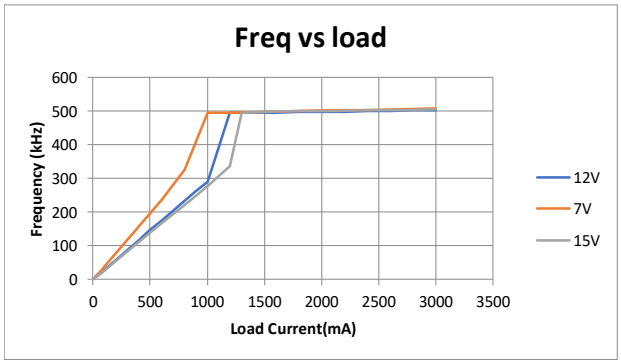


Figure 39. V_{OUT} Ripple at I_{OUT} = 3A (V_{OUT}=5V)

7. Functional Description

The RAA211230 is an integrated synchronous buck regulator with constant on time (COT) current mode control. It can operate across a wide input voltage range from 4.5V to 24V delivering load current up to 3A across the -40°C to 125°C temperature range. The output voltage is sensed on the FB pin through external feedback resistors and compared with the internal reference of 0.768V to produce the control signal which in turn decides when to turn on the high side FET. The internal Constant On-Time circuit decides the on-time of the high side FET based one the sensed valued of Vin and Vout.

At low load conditions, the regulator operates in DCM mode with frequency varying as per the output load (Pulse-frequency modulation). At higher loads, the part transitions to CCM mode with constant frequency of 500kHz.

7.1 Soft-Start

Soft-start forces the regulator to ramp up in a controlled fashion, which prevents high inrush current or output voltage overshoot at startup. During soft-start, the reference voltage input of the error amplifier ramps up from 0V to its nominal value of 0.768V in 1ms.

7.2 Undervoltage Lockout

The regulator has Undervoltage lockout (UVLO) on VIN pin. It prevents the regulator from starting up until the input voltage exceeds 4.45V (typical). The UVLO threshold has approximately 250mV of hysteresis, therefore the device continues to operate when Vin decreases until it drops below 4.2V (typical). Hysteresis prevents the part from turning off during power-up if the Vin is non-monotic.

7.3 Enable Control

RAA211230 has an enable pin, which turns the device on when pulled high. When EN is low, the IC goes into shutdown mode. RAA211230 has a EN rising threshold voltage of 1.29V and EN threshold of hysteresis of 0.1V.

EN pin can be tied directly to VIN for “always-on” operation. The device has a very accurate Enable threshold, which allows the user to program the VIN UVLO, by connecting VIN to EN through a resistor divider. The UVLO can be set with the resistor divider based on the following equation (see Figure 2.)

(EQ. 1) $$\frac{REN1}{REN2} = \frac{VINR - 1.29}{1.29}$$

Where V_{INR} is the rising threshold of VIN UVLO. The resulting input voltage () for the part to be turned off would is calculated as:

(EQ. 2) $$VINF = 1.28X\frac{REN1 + REN2}{REN2}$$

7.4 Overcurrent Protection (OCP) and V_{OUT} Undervoltage Protection

RAA211230 has Low-Side Overcurrent (LSOC) Protection feature. After the regulator starts up, if the current through the internal low-side MOSFET is over the current limit, the device skips the high-side cycles until the LSOC condition clears.

RAA211230 also has a V_{OUT} Undervoltage (UV) protection. The internal under-voltage comparator compares the FB pin voltage to 65% of the reference voltage. When this voltage drops below 65% of nominal (because of a drop of VOUT to below 65% of its set point), the regulator stops switching and engages Hiccup mode operation at an interval of 15ms.

7.5 Over-temperature Protection

Over-temperature protection (OTP) limits the maximum junction temperature in the RAA211230. This limits total power dissipation by shutting off the regulator when the IC junction temperature exceeds 170°C (typical). There is a 20°C hysteresis for OTP. After the junction temperature drops below 150°C, the RAA211230 resumes operation by stepping through soft-start.

8. Applications Information

The recommended component selections for typical applications are listed in Table 1.

Table 1. Recommended Components Selection for Typical Application

V_{IN}(V)	V_{OUT}(V)	R_{FB1}(kΩ)	$R_{FB2(}$kΩ)	L(µH)	C_{OUT}(µF)
12	1.8	26.8	20	2.2	100
12	3.3	65.9	20	3.3	47
12	5	110.2	20	4.7	44
12	8	188.3	20	4.7	22

8.1 Inductor Selection (see table 1)

8.2 Input Capacitor Selection (refer to evaluation board guide)

8.3 Output Capacitor Selection (see table 1)

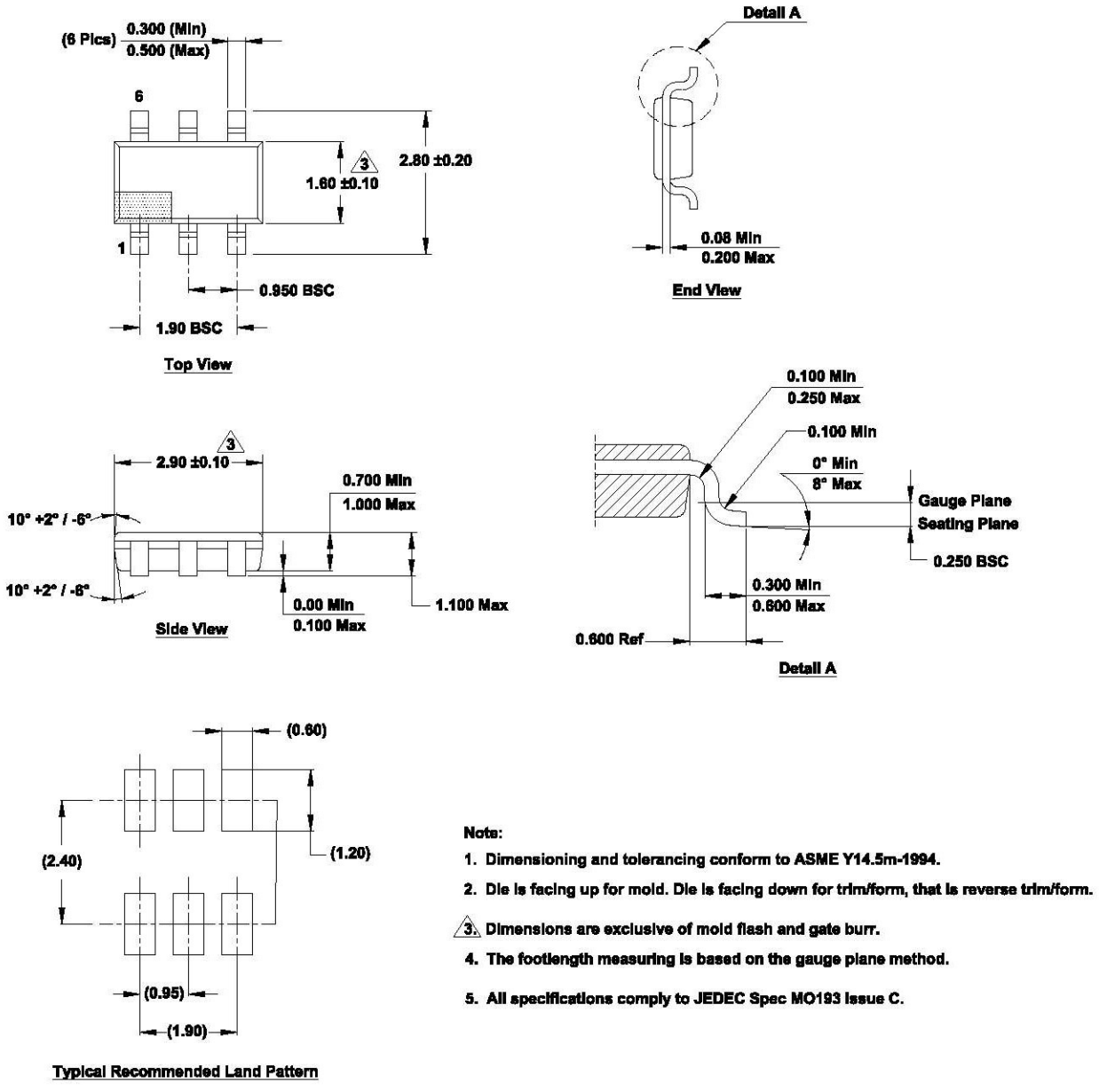
8.4 BST Refresh description

8.5 Boot Capacitor Selection, use 0.1uF MLCC capacitor

9. Package Outline Drawing

For the most recent package outline drawing, see P6.064C.

P6.064C
6 Lead Thin Small Outline Transistor (TSOT) Plastic Package
Rev 2, 12/20



Note:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. Die is facing up for mold. Die is facing down for trim/form, that is reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specifications comply to JEDEC Spec MO193 Issue C.

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
RAA2112304GP3#JA0	TBD	6Ld TSOT-23	P6.064C	Reel, 3k	-40 to +125°C

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA211230 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

11. Revision History

Rev.	Date	Description
0.04	Nov 8, 2021	Minor update.
0.03	Oct 28, 2021	Updated Figures 1 and 2. Updated BST maximum value in Abs Max section. Updated the Enable Voltage section in the Electrical specifications table. Updated Thermal Shutdown spec to 170C.
0.02	Sep 21, 2021	Updated the ordering information table. Other minor updates.
0.01	Jan 13, 2021	Initial preliminary release