



ASNT5040-PQC is available on two evaluation boards: one with negative supply and one with positive supply. Application notes for these two evaluation boards are presented in order of:

- Negative supply on ASNT05_12
- Positive supply on ASNT05_11

By default, ADSANTEC will ship the positive supply evaluation board. Please send us a message through the DigiKey marketplace website if you would like to receive the negative supply version.

The datasheet for ASNT5040-PQC can be accessed through the following [LINK](#).



ASNT5040-PQC on ASNT05_12 Evaluation Board DC-17GHz XOR Logic Gate Application Note

Part Description

The ASNT5040-PQC XOR logic gate accepts broadband data and clock signals at its two differential input ports *dap/dan* and *dbp/dbn* and delivers the result of the Exclusive-OR (XOR) Boolean logic function to its differential output port *qp/qn*.

The part is mounted on an ASNT05_12 evaluation board with *50Ohm* transmission lines to transfer signals to/from the chip to 6 high-speed edge-mount female connectors (Southwest or similar) as shown in Fig. 1. The board has a MOLEX connector for the power supply, as well as signal filters, supply filters, and decoupling networks. The board measures approximately 2.0x2.0 inches, without connectors.

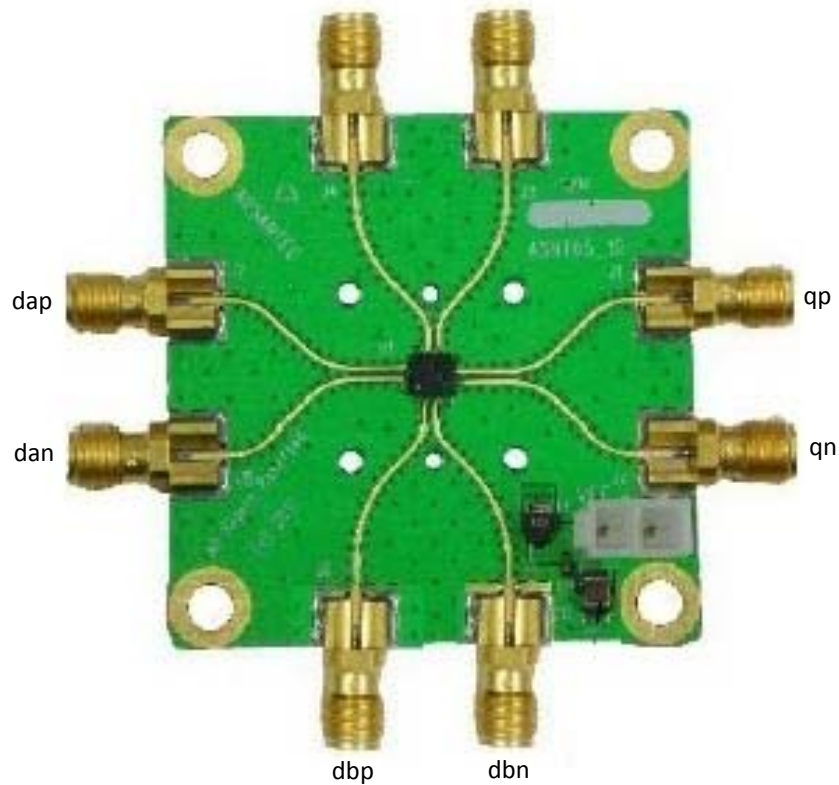


Fig. 1. Layout of ASNT05_12 PCB

The signal and power connectors are described in Table 1 and Table 2 below.

Table 1. Signal Connectors

Name on PCB	Name on Chip	Signal description	Signal polarity	I/O type
J7	dap	Differential data/clock inputs with internal SE 50Ohm termination to VCC	Direct	CML input
J8	dan		Inverted	
J1	qp	Differential outputs with internal SE 50Ohm termination to VCC; require external SE 50Ohm termination to VCC	Direct	CML output
J2	qn		Inverted	
J6	dbp	Differential data/clock inputs with internal SE 50Ohm termination to VCC	Direct	CML input
J5	dbn		Inverted	

Table 2. Power Supply Connectors

Name on PCB	Name on Chip	Supply type	Supply voltage, V
GND	vcc	External ground	0
VEE	vee	Main negative power supply	-3.3

Initial Setup and Basic Functionality

1. The part is static sensitive. **Please observe anti-static protection procedures!**
2. Measure the resistance of all connector pins to VCC, including the power supply, while making sure the board is grounded. All I/O ports should measure 50Ohms while on the power supply connector, VEE should be high impedance and GND should be a short. Fig. 2 shows the resistance values of the described I/O connectors.

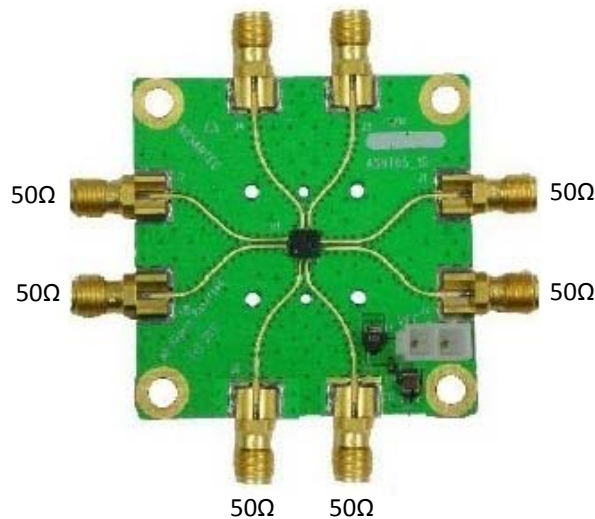


Fig. 2. Impedance of I/O Connectors



3. Switch on the first external power supply unit and set it to a negative supply voltage with a value of $-0.0V$ (**positive output pin of the unit must be shorted to ground**).
4. Connect the supply unit's output pins to the PCB's Molex connector marked VEE GND so that the negative output pin is connected to VEE connector pin.
5. Gradually increase the negative supply voltage to $-3.3V$.
6. Monitor the supply current in accordance with the part's specifications.
7. Apply a differential or SE high-speed data or clock signal to connectors J7/J8. **DC blocks or the appropriate shift of voltage levels may be required!**
8. Apply a differential or SE high-speed data or clock signal to connectors J6/J5. **DC blocks or the appropriate shift of voltage levels may be required!**
9. Observe a high-speed XOR logic signal at connectors J1/J2. Connect them to an oscilloscope or similar device with 50Ω termination to ground either directly or through DC blocks. If the correct logic of the two input signals is not observed, adjust the phase of one of the inputs accordingly.

Board Dimension

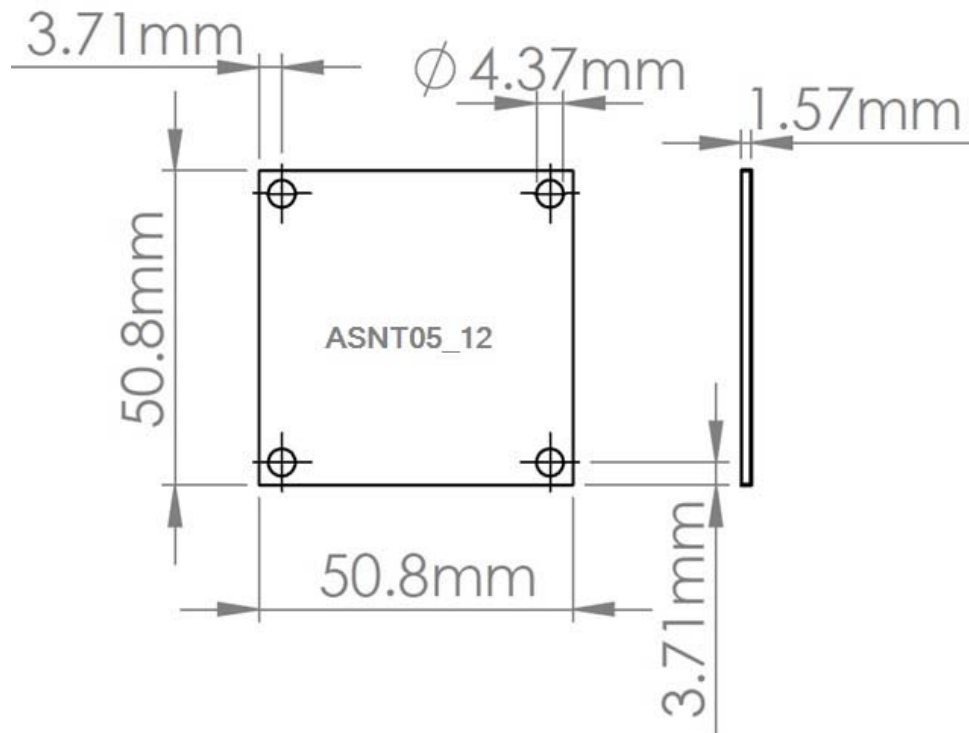


Fig. 3. ASNT05_12 Board Dimensions



ASNT5040-PQC on ASNT05_11 Evaluation Board DC-17GHz XOR Logic Gate Application Note

Part Description

The ASNT5040-PQC XOR logic gate accepts broadband data and clock signals at its two differential input ports *dap/dan* and *dbp/dbn* and delivers the result of the Exclusive-OR (XOR) Boolean logic function to its differential output port *qp/qn*.

The part is mounted on an ASNT05_11 evaluation board with 50Ω transmission lines to transfer signals to/from the chip to 6 high-speed edge-mount female connectors (Southwest or similar) as shown in Fig. 4. The board has a MOLEX connector for the power supply, as well as signal filters, supply filters, and decoupling networks. The board measures approximately 2.0x2.0 inches, without connectors.

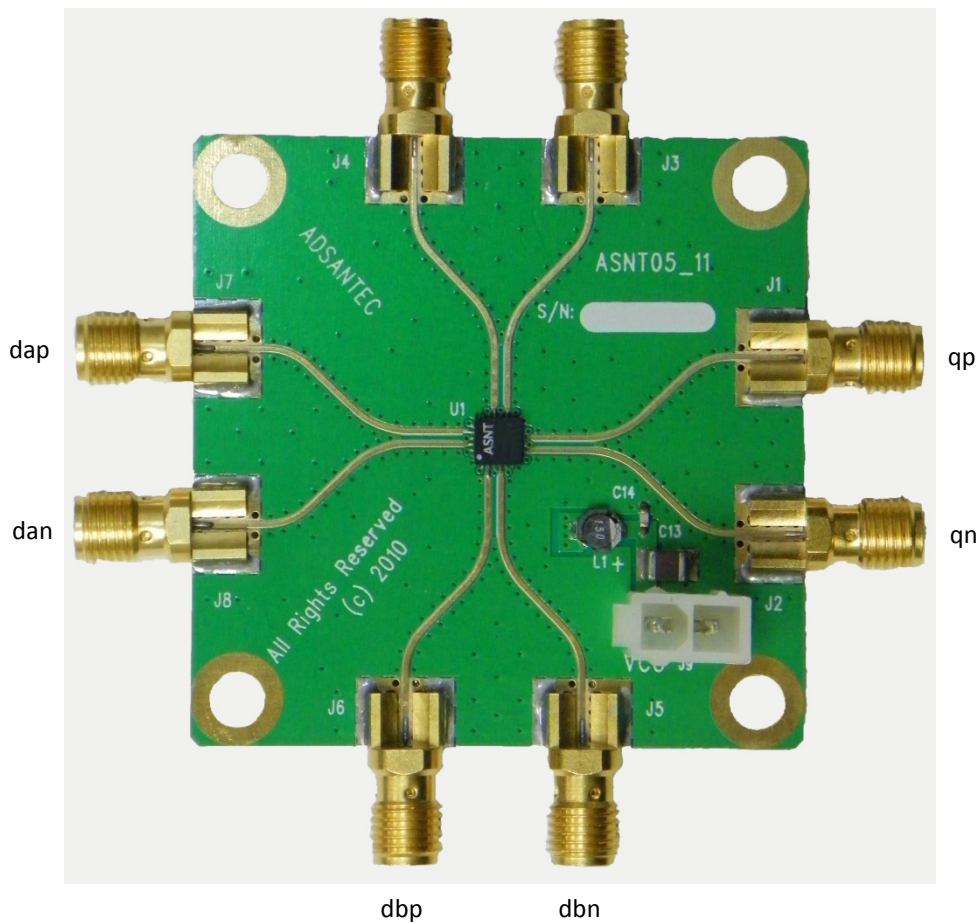


Fig. 4. Layout of ASNT05_11 PCB

The signal and power connectors are described in Table 1 and Table 2 below.

Table 3. Signal Connectors

Name on PCB	Name on Chip	Signal description	Signal polarity	I/O type
J7	dap	Differential data/clock inputs with internal SE 50 Ω termination to VCC	Direct	CML input
J8	dan		Inverted	
J1	qp	Differential outputs with internal SE 50 Ω termination to VCC; require external SE 50 Ω termination to VCC	Direct	CML output
J2	qn		Inverted	
J6	dbp	Differential data/clock inputs with internal SE 50 Ω termination to VCC	Direct	CML input
J5	dbn		Inverted	

Table 4. Power Supply Connectors

Name on PCB	Name on Chip	Supply type	Supply voltage, V
VCC	vcc	Main positive power supply	+3.3
GND	vee	External ground	0

Initial Setup and Basic Functionality

- The part is static sensitive. **Please observe anti-static protection procedures!**
- Measure the resistance of all connector pins to VCC, including the power supply, while making sure the board is grounded. All I/O ports should measure 50 Ω while on the power supply connector, VCC should be a short, and GND should be high impedance. Fig. 5 shows the resistance values of the described I/O connectors.

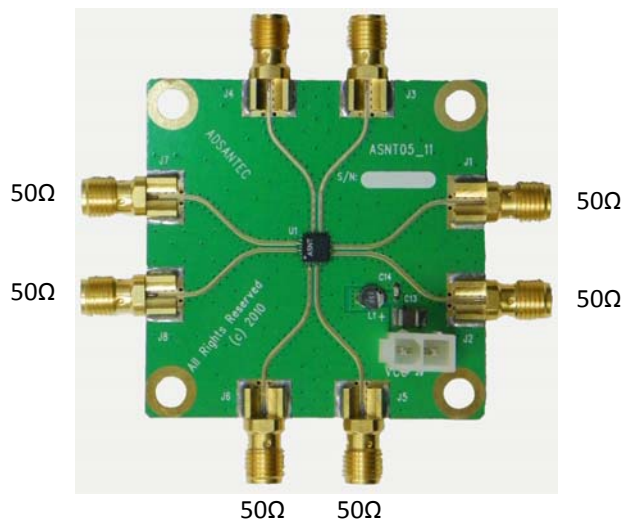


Fig. 5. Impedance of I/O Connectors

12. Switch on the first external power supply unit and set it to a positive supply voltage with a value of +0.0V (negative output pin of the unit must be shorted to ground).
13. Connect the supply unit's output pins to the PCB's Molex connector marked VCC GND so that the positive output pin is connected to VCC connector pin.
14. Gradually increase the positive supply voltage to +3.3V.
15. Monitor the supply current in accordance with the part's specifications. Current should be approximately 125mA.
16. Apply a differential or SE high-speed data or clock signal to connectors J7/J8. DC blocks or the appropriate shift of voltage levels may be required!
17. Apply a differential or SE high-speed data or clock signal to connectors J6/J5. DC blocks or the appropriate shift of voltage levels may be required!
18. Observe a high-speed XOR logic signal at connectors J1/J2. Connect them to an oscilloscope or similar device with 50Ohm termination to ground through DC blocks. If the correct logic of the two input signals is not observed, adjust the phase of one of the inputs accordingly.

Board Dimensions

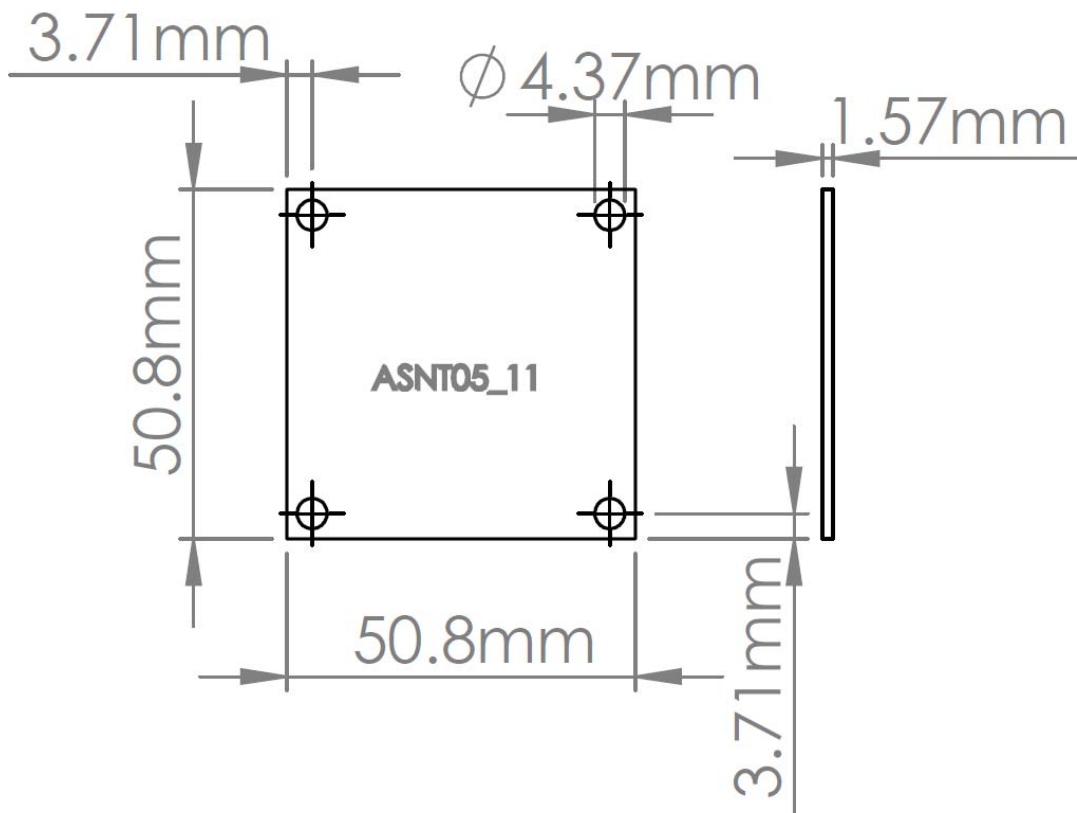


Fig. 6. ASNT05_11 Board Dimensions



ADSANTEC

Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Dr., Ste #112, Torrance, CA 90505

Office: (310) 530-9400 Fax: (310) 530-9402
www.adsantec.com

Revision History

Revision	Date	Changes
1.0.1	09-2020	Initial Release



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