User's Guide

SPRUIF9–August 2017

EtherCAT® Interface for High-Performance C2000™ MCU

This reference design demonstrates how to connect an EtherCAT ET1100 slave controller to a C2000 Delfino™ MCU. The interface supports both de-multiplexed address/data busses for maximum bandwidth and minimum latency, and a serial peripheral interface (SPI) mode for low pin-count EtherCAT communication. The slave controller offloads the processing of 100 Mbps Ethernet-based fieldbus communication, thereby, eliminating CPU overhead for these tasks.

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Trademarks

1 Introduction

1.1 Features

- High-Performance Real-Time Control MCU Paired With Low-Latency Ethernet-Based Communication
- High-Bandwidth, Low-Latency Interface to Beckhoff ET1100 EtherCAT Slave Controller
- Supports Both Asynchronous Parallel and SPI Connections
- Glueless Interface
- Eliminates CPU Overhead for EtherCAT Frame Processing

1.2 Applications

- Industrial Drives
- Servo Motor Drives
- Manufacturing Robotics
- CNC Machinery
- Remote I/O

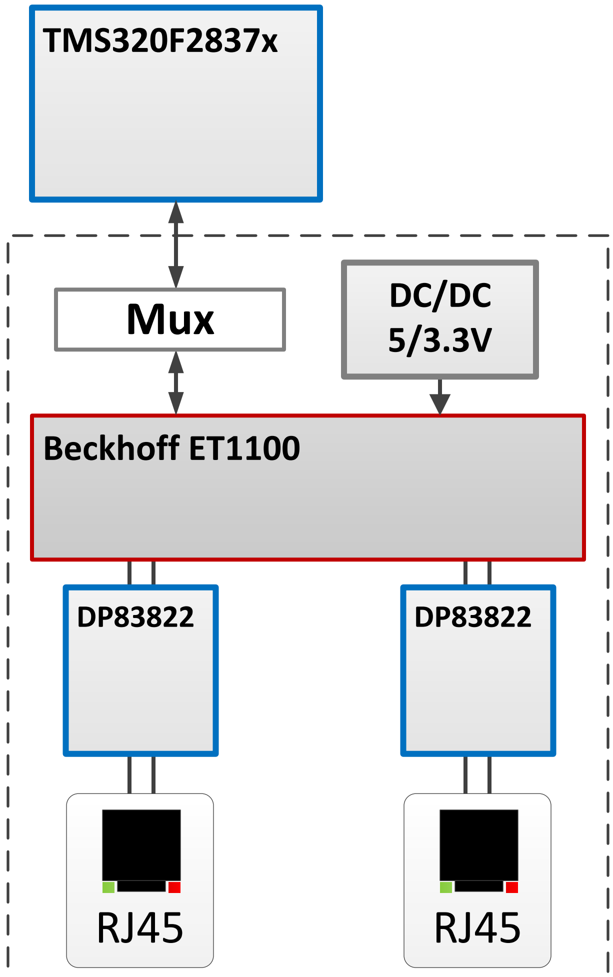

Figure 1. TMDSECATCNCD379D Block Diagram

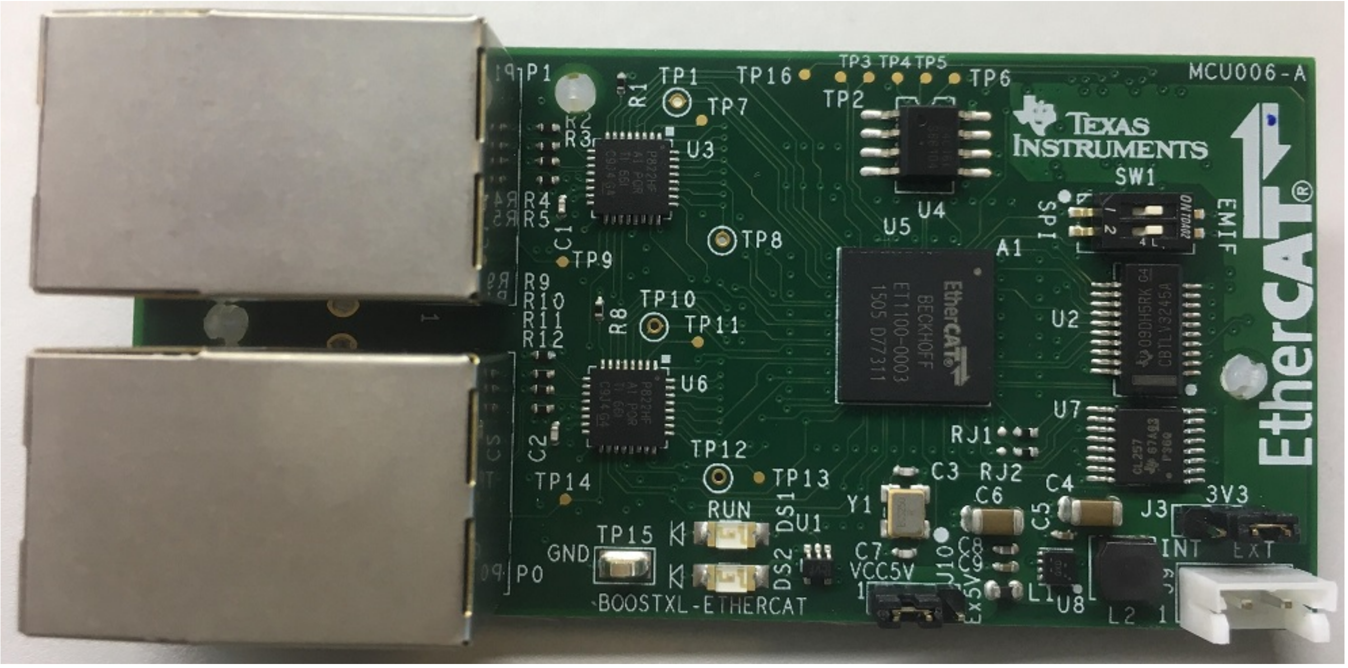

Figure 2. TMDSECATCNCD379D Adapter Board

1.3 *DesignDRIVE*

For more information on DesignDRIVE technology for industrial drive applications, see the following links:

- http://www.ti.com/c2000drives
- http://training.ti.com/c2000-designdrive
- http://www.ti.com/tool/designdrive

2 System Overview

2.1 *System Description*

The TMDSECATCNCD reference design is an adapter board for TI F2837x controlCARDs. When coupled with a C2000 MCU, it uses a Beckhoff ET1100 EtherCAT Slave Controller (ESC) and TI Ethernet PHYs to enable the creation of EtherCAT slave nodes. The adapter board format uses a 60-pin high-density connector that can support both asynchronous parallel and SPI interfaces.

This user's guide illustrates how to set up the EtherCAT adapter board module, initialize the ET1100 subsystem for first use, and install and configure the Beckhoff TwinCAT 3 software for use as an EtherCAT master in a test setup. Example code is provided to configure both SPI and external memory interface (EMIF) interfaces and run simple read and write tests across an EtherCAT network.

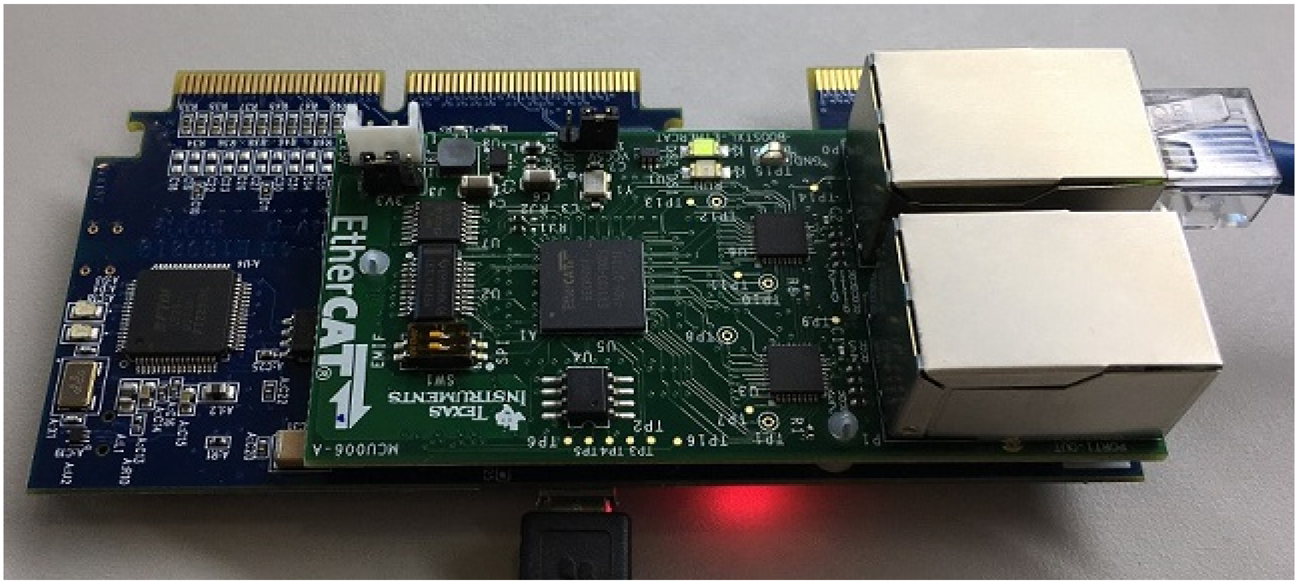

Figure 3. TMDSECATCNCD379D controlCARD and Adapter Board

2.2 Key System Specifications

Table 1. EMIF Configuration and Timing Settings for ET1100 PDI

PARAMETER	DESCRIPTION	VALUE	DELAY [1]
TA	Read-to-Write Turnaround time	1	5 ns
RHOLD	Address and CSn hold after OEn LH edge	1	5 ns
RSTROBE	Read Strobe time in units of EMIF Clocks	64	320 ns
RSETUP	Address and CSn to OEn assertion delay	1	5 ns
WHOLD	Write Hold time after WE deassertion	1	5 ns
WSTROBE	Write Strobe (WE) width	2	10 ns
WSETUP	Address and CSn setup time to WE assertion	1	5 ns
EW	Extended Wait Mode	ENABLE	-
SS	Strobe Select Mode	DISABLE	-

(1) F2837x system with Fsysclk = 200 MHz.

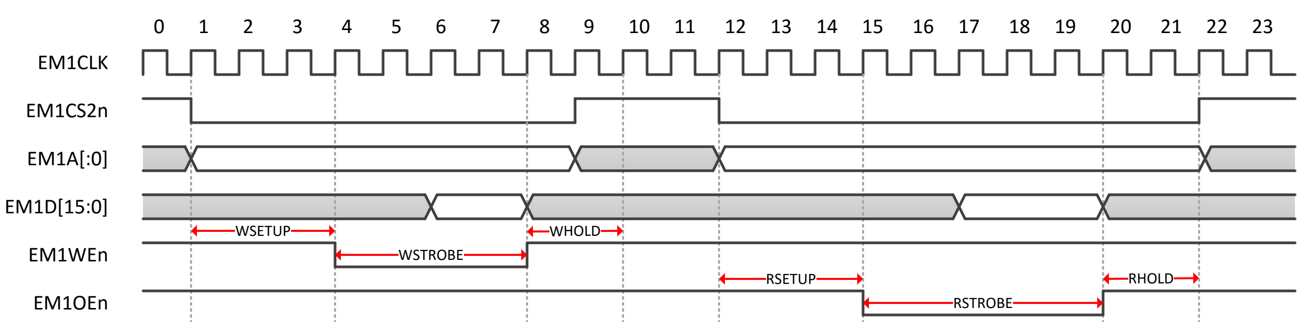

Figure 4. EMIF PDI Timing Diagram

2.3 Block Diagram

Figure 6 shows the block diagram of the SPI and EMIF interfaces. In both configurations, the F2837x runs the EtherCAT slave stack while the ET1100 is used to offload the EtherCAT Slave Controller (ESC) frame processing, FMMU, and SyncManager operations.

Certain pins on the ET1100 are used on both the SPI and asynchronous interfaces, which requires the SN74CBTLV3257 mux and SN74CBTLV3245 buffer to steer these signals to the appropriate GPIO on the F2837x MCU.

The EtherCAT adapter board features an on-board DC-DC 5V–3.3V converter, which allows the 3.3V VDD to be either sourced from the C2000 controlCARD or generated locally from an off-board 5V source.

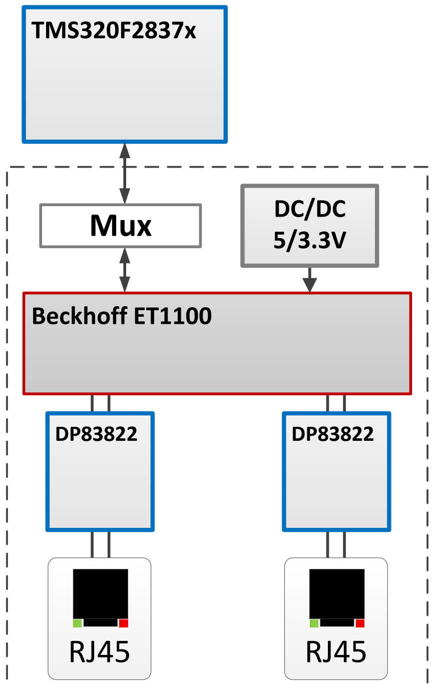

Figure 5. Block Diagram

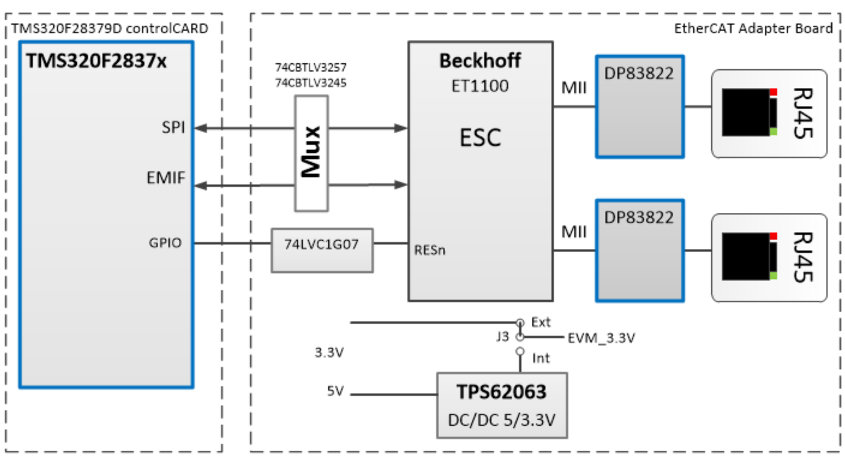

Figure 6. F2837x SPI and EMIF Connections to the EtherCAT Slave Controller

2.4 Highlighted Products

2.4.1 TMS320F28379D

The Delfino TMS320F2837x is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications such as industrial drives and servo motor control; solar inverters and converters; digital power; transportation; and power line communications. Complete development packages for digital power and industrial drives are available as part of the powerSUITE and DesignDRIVE initiatives. The F2837x supports a new dual-core C28x architecture that significantly boosts system performance while integrated analog and control peripherals allow designers to consolidate control architectures and eliminate multiprocessor use in high-end systems.

In the TMDSECATCNCD379D design, the F2837x receives EtherCAT data from the ET1100 through either a serial (SPI) interface or an asynchronous parallel memory interface (EMIF). Figure 7 shows the use of EMIF2, but either EMIF can be used to interface to the ET1100. Note that GPIOs 93 and 94 are for future expansion to address a larger memory space. They are not used in the example code.

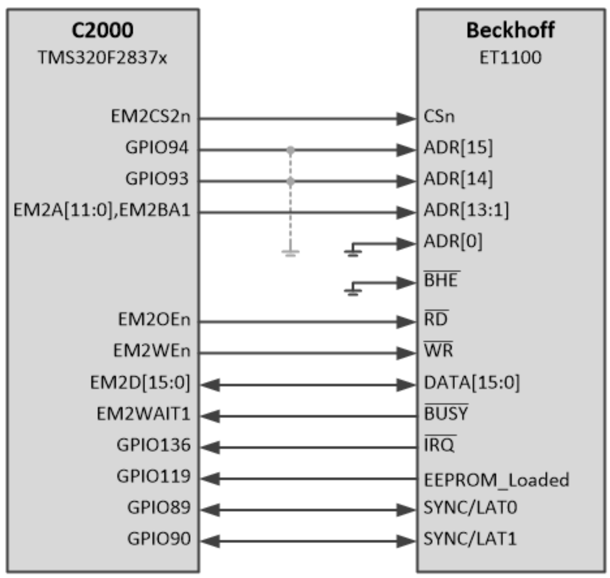

Figure 7. EMIF Interface to ET1100 EtherCAT Slave Controller

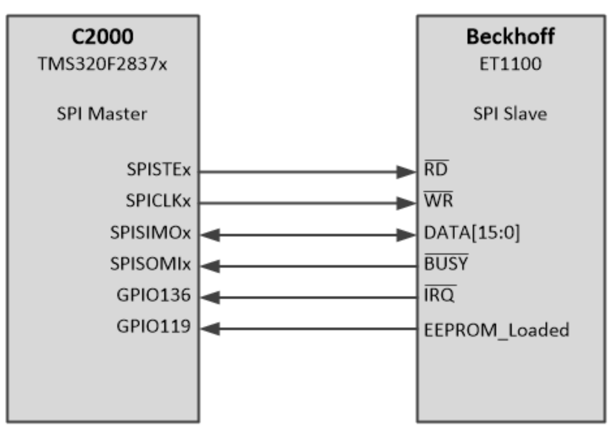

Figure 8. SPI Interface to ET1100 EtherCAT Slave Controller

2.4.2 DP83822

The DP83822 is a low power single-port 10/100 Mbps Ethernet PHY. It provides all physical layer functions needed to transmit and receive data over both standard twisted-pair cables or connect to an external fiber optic transceiver. Additionally, the DP83822 provides flexibility to connect to a MAC through a standard MII, RMII or RGMII interface.

2.4.3 TPS62063

The TPS6206x is a family of highly efficient synchronous step-down DC-DC converters. They provide up to 1.6-A output current. With an input voltage range of 2.7-V to 6-V, the device is a perfect fit for power conversion from 5-V or 3.3-V system supply rails. The TPS6206x operates at 3-MHz fixed frequency and enters power save mode operation at light load currents to maintain high efficiency over the entire load current range. The power save mode is optimized for low-output voltage ripple. For low noise applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high.

In this reference design, the converter enables power to be supplied from either the controlCARD or an external 5-V source.

2.4.4 SN74LVC1G07

This single buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation. The output of the SN74LVC1G07 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

In this design, the open-drain buffer connects a GPIO from the F28379D controlCARD to the ET1100 EtherCAT slave controller reset pin, thereby, enabling independent reset of both devices.

2.4.5 SN74CBTLV3245A

The SN74CBTLV3245A provides eight bits of high-speed bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as one 8-bit switch. When output enable (OE) is low, the 8-bit bus switch is on, and port A is connected to port B. When OE is high, the switch is open and the high-impedance state exists between the two ports.

In this TI Design, the bus switch isolates selected ET1100 outputs from the F28379D controlCARD GPIOs when the EMIF interface is not used (SPI mode). Note that the bus switches are optional in a design using only a single interface type.

2.4.6 SN74CBTLV3257

The SN74CBTLV3257 device is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable (OE) input is high.

This multiplexer connects selected GPIOs to the ET1100 depending on the interface mode (EMIF or SPI). Note that the multiplexer is optional in a design using only a single interface type.

2.4.6.1 Beckhoff ET1100 EtherCAT Slave Controller (ESC)

The ET1100 device is an EtherCAT Slave Controller (ESC). It handles all communications between the EtherCAT fieldbus and the F2837x interface (either SPI or EMIF).

For more information, see http://www.beckhoff.com.

2.4.7 TMS320F2837xD Delfino Microcontroller Functional Diagram

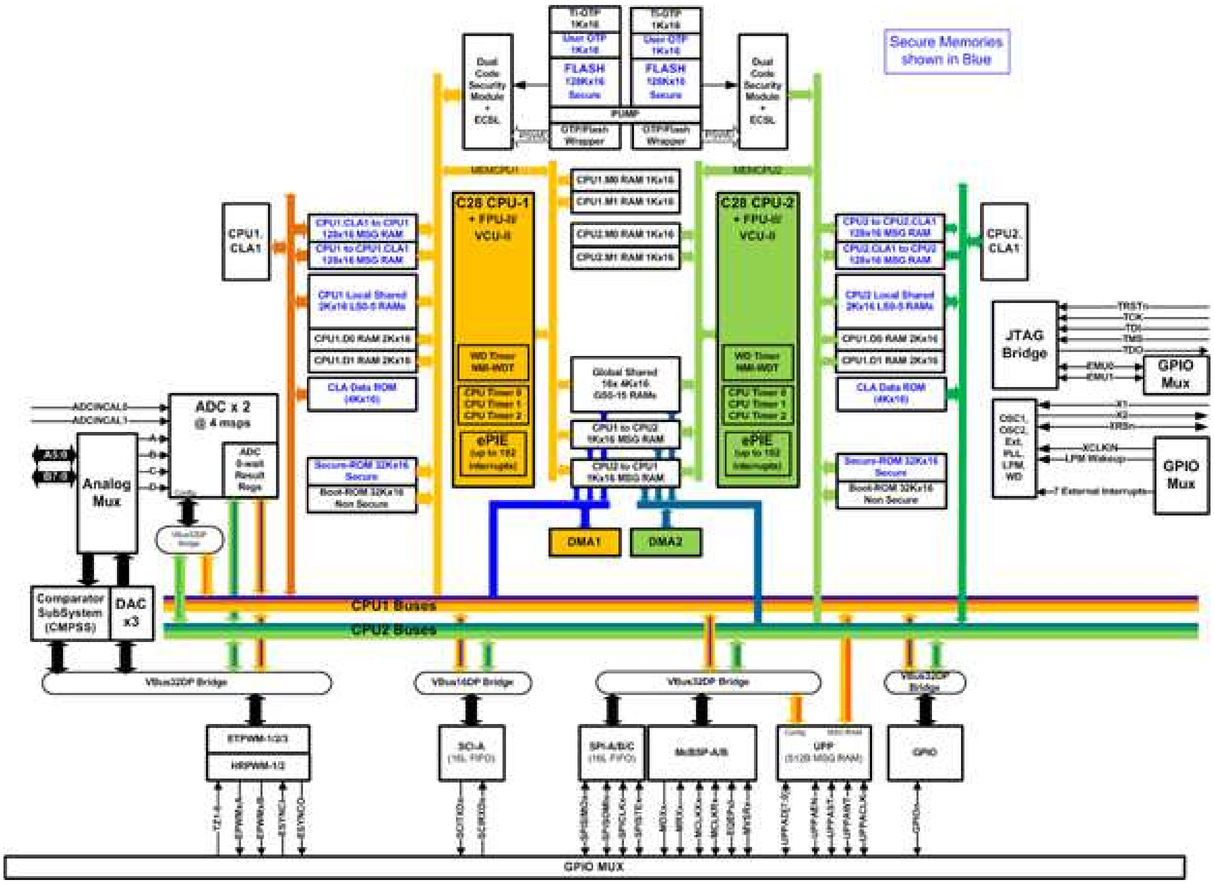

Figure 9. TMS320F2837xD Functional Diagram

2.4.8 Ethernet PHY Functional Diagram

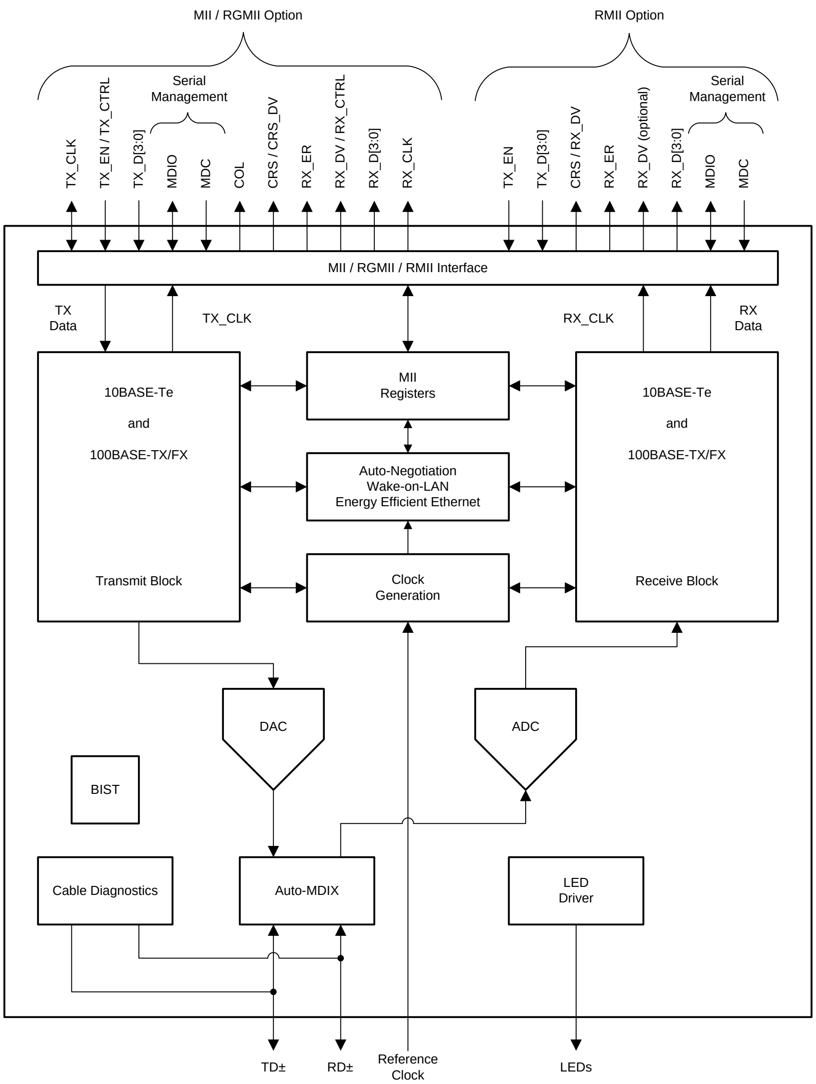

Figure 10. DP83822 Functional Diagram

2.4.9 SN74CBTLV3245A Functional Diagram

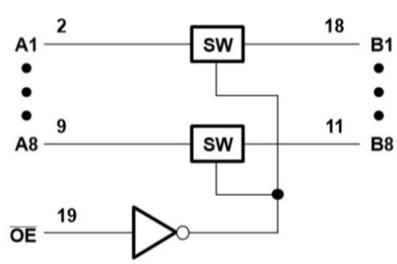

Figure 11. SN74CBTLV3245A Functional Diagram

2.4.10 SN74CBTLV3257 Functional Diagram

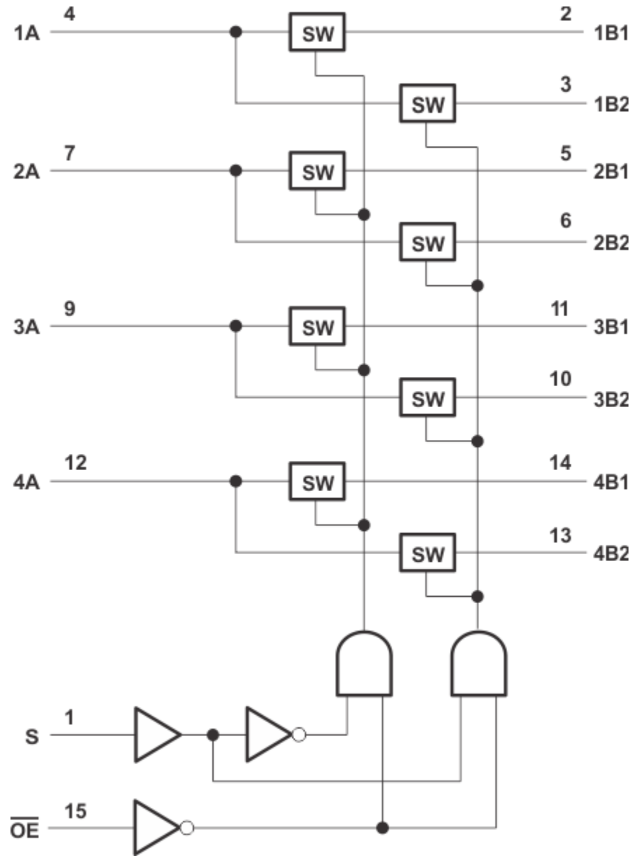

Figure 12. SN74CBTLV3257 Functional Diagram

2.4.11 ET1100 Functional Diagram

Bechoff data sheet: http://download.beckhoff.com/download/document/io/ethercat-development-products/ethercat_et1100_datasheet_v1i9.pdf.

3 Getting Started (Hardware)

This document describes an F28379D controlCARD adapter board. The adapter board can support either an EMIF or an SPI interface.

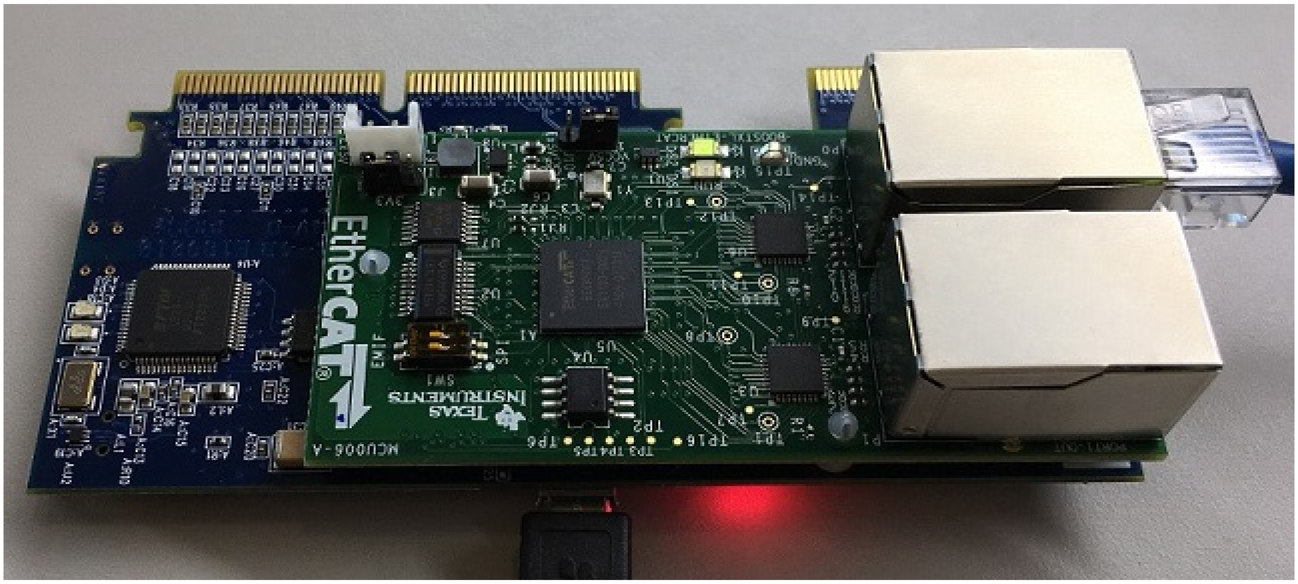

Figure 13. Stacked F28379D ControlCard + EtherCAT Adapter Board

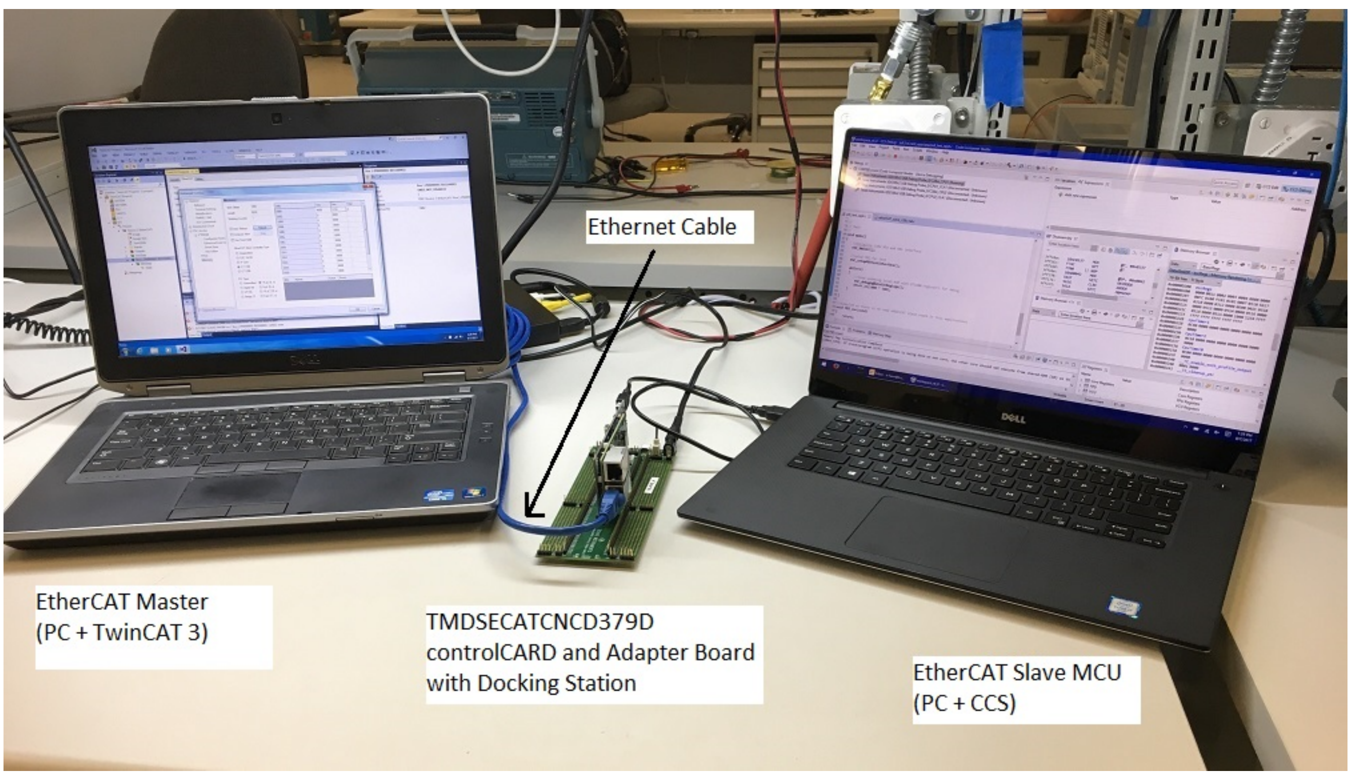

Figure 14. EtherCAT Test Setup

3.1 EtherCAT Master Configuration Using TwinCAT3

3.1.1 Download and Install TwinCAT3 From the Beckhoff website

The TwinCAT3 software is available from the Beckhoff website at http://www.beckhoff.com. Follow the left sidebar to Download → Software → TwinCAT 3 → TE1xxx | Engineering. As of this writing, the most recent version of this software is TwinCAT 3.1 – eXtended Automation Engineering (XAE) v 3.1.4022.0.

3.1.2 Verify the TwinCAT Runtime is Active

1. Check for the EtherCAT icon in the notification panel in the lower-right corner as shown in Figure 15. If this is absent, open the notification panel and check in the popup window for the TCSwitchRuntime. Right click on this icon and select Tools → TCSwitchRuntime.

Figure 15. TwinCAT Runtime Icon in Windows Toolbar

2. Verify that the TCSwitch Runtime is active. The “Deactivate” button should be showing as illustrated in Figure 16. If this button reads “Activate”, click that button to start the TCSwitchRuntime.

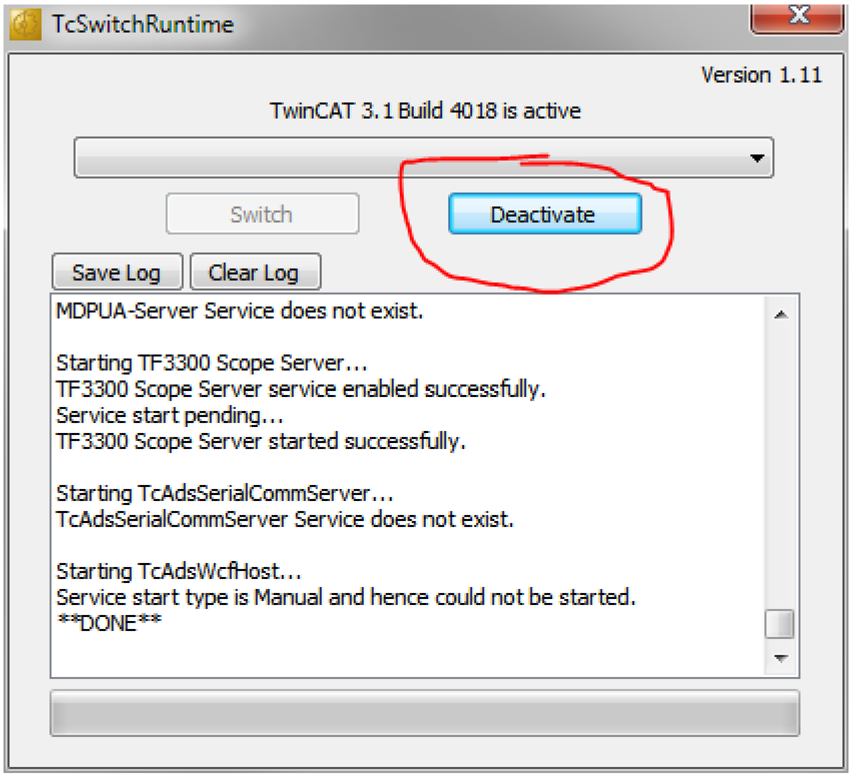

Figure 16. TwinCAT Runtime Dialog Box

3. If the TCSwitchRuntime is not found in steps 1 and 2 above, then locate the runtime in the file system. A typical location is: “C:\TwinCAT\TcSwitchRuntime\TcSwitchRuntime.exe”. Note that it is NOT commonly found in the Start Menu.

3.2 Start TwinCAT3 and Verify That TwinCAT is Running in Visual Studio

1. Locate the TwinCAT XAE, which can be found in one of three places:

   (a) Start menu → under Beckhoff → TwinCAT3 → TwinCAT XAE (VS 2010).

   (b) Desktop icon is shown in Figure 17.

Figure 17. TwinCAT3 XAE Desktop Icon

   (c) Notification panel icon → right click and select TwinCAT XAE (VS 2010).

Figure 18. TwinCAT3 Icon in Toolbar

2. Verify that TwinCAT is running under Visual Studio. “TwinCAT” and “PLC” should both appear in the main toolbar as shown in 1. If these menu items are not shown, then the TC3 runtime is NOT running. Go back to step Figure 19 to restart the TC3 runtime.

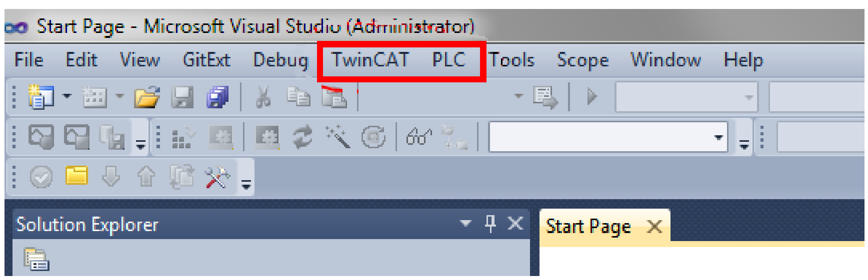

Figure 19. Visual Studio Menus for TwinCAT3

3. Open a new EtherCAT project.

   (a) File → New → Project.

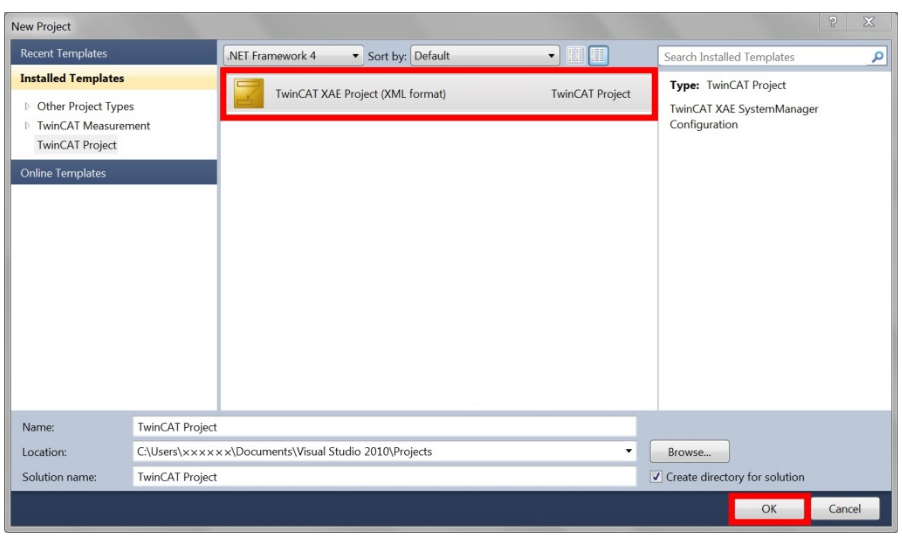

Figure 20. TwinCAT3 New Project Dialog

4. Verify that a Realtime Ethernet Adapter is installed.
   (a) TwinCAT → Show Realtime Ethernet Compatible Devices
   If no RT adapter is installed, select one from the list of Compatible devices and click “Install”, then exit this popup.

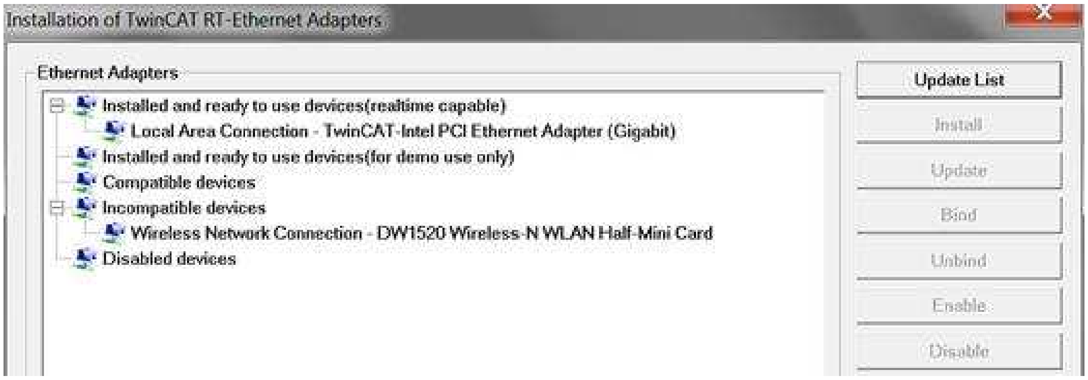

Figure 21. TwinCAT3 EtherNet Adapter Dialog

5. Scan for the newly installed Realtime adapter by clicking TwinCAT → Scan.
   (a) A popup indicating TwinCAT has found the adapter that should appear (see Figure 22).

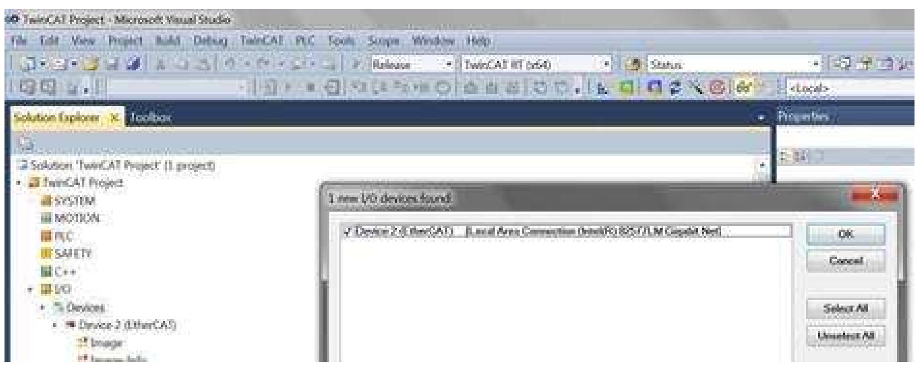

Figure 22. TwinCAT3 Discovery of Ethernet Adapter

   (b) Click “OK”, then click “Yes” to the following two popups (see Figure 23).

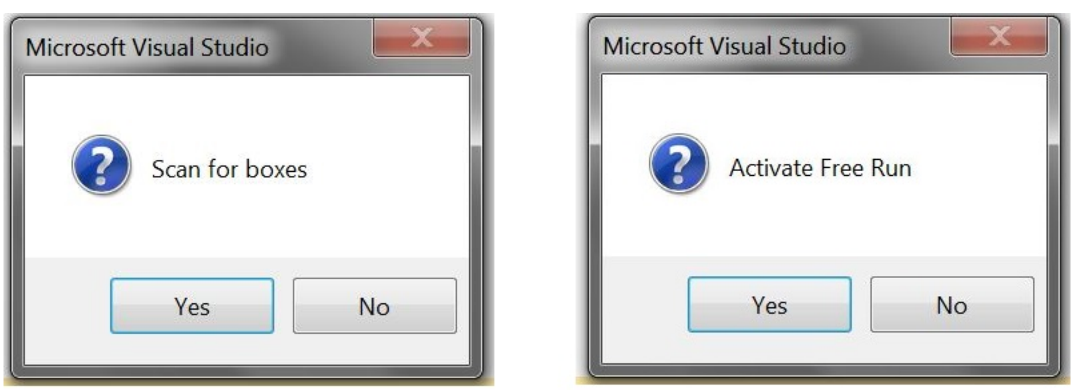

Figure 23. TwinCAT3 Master Scan for Slaves and Free Run Activation

(c) The screen view shown in Figure 24 should now be visible in TwinCAT3, indicating that the Master and Slave are connected and prepared for use. Note that “Box 1” appears at the bottom of the image, indicating that TwinCAT has discovered the EtherCAT slave. If this is the first time that the slave has been connected and the EEPROM has not yet been programmed, the “Box n ()” label (for example, “TI_C2KESC”) will not be visible.

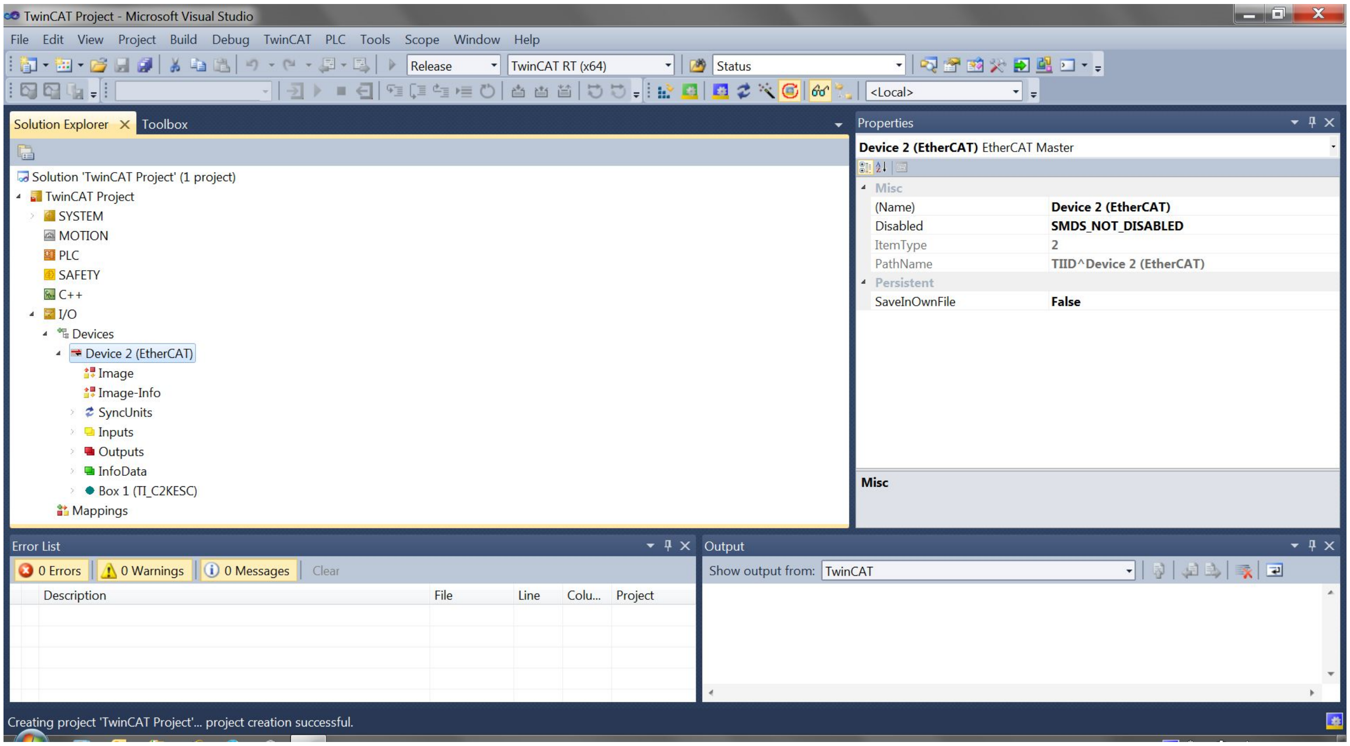

Figure 24. TwinCAT Solution Explorer Showing EtherCAT Master (Device 2) and Slave (Box1, TI_C2kESC)

6. The EtherCAT Master is now ready for communication with the Slave device.

3.3 Configuring the EtherCAT Adapter Board Interface for EMIF or SPI Operation

The EtherCAT adapter board must be configured prior to power-up to select between the EMIF or SPI interface from the C28x to the ET1100 slave controller. Options for power source and interface type are available through jumpers and/or DIP switches as described in Figure 25 and Table 2.

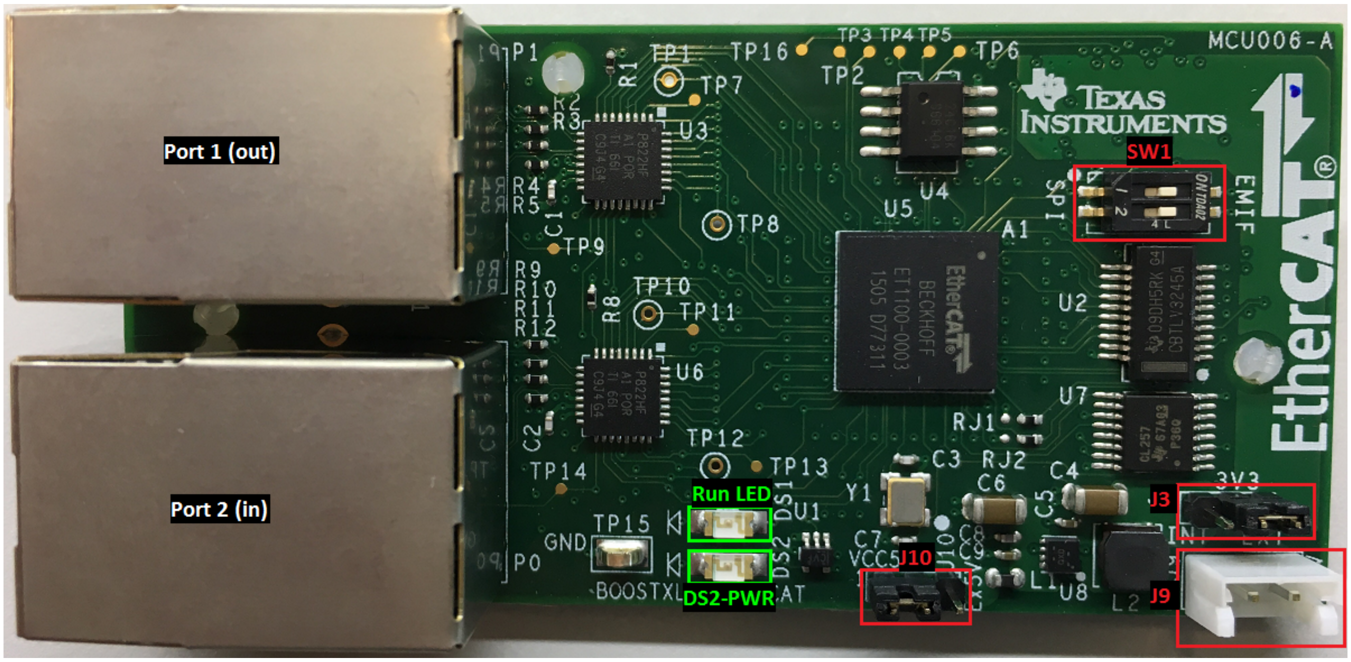

Figure 25. EtherCAT Adapter Board LED and Switch Locations

Table 2. EtherCAT LED and Switch Usage Descriptions

NAME	OPTIONS	DESCRIPTION
Switches/Jumpers		
SW1	L – SPI R – EMIF	Selects between EMIF and SPI Interface Modes
J3	1-2 off-board 2-3 on-board	Off-board: 3.3 V is provided directly from attached controlCARD On-board: 3.3 V is generated by the on-board regulator from a separate 5 V supply.
LEDs		
RUN LED	State Machine Status [(1)]	Off: ET1100 Device is in INIT state. On: ET1100 Device is in Operational state.
DS2/PWR LED	3.3 V Power	ON indicates 3.3 V is being supplied to the board. For details, see the schematics in Figure 38.

(1) Additional RUN LED states provided in the *ET1100 Digital I/O Signals* table of the ET1100 data sheet, which is located at: http://download.beckhoff.com/download/document/io/ethercat-development-products/ethercat_et1100_datasheet_v1i9.pdf.

3.4 Preparing the Adapter Board for EtherCAT Communcation Using TwinCAT3

After installing the TwinCAT3 software in the previous section and verifying connectivity between the EtherCAT Master and the slave node, the ESC EEPROM must be programmed to enable communication to the C28x device over either the EMIF or SPI PDI. The following procedure writes the binary file associated with the selected PDI type into the EEPROM:

1. After starting up the TwinCAT software in Section 3.1, the screen should look something like Figure 26. Double clicking the EtherCAT slave (labelled “Box 1” in the figure) brings up the EtherCAT properties window on the right. Click “Advanced Settings”.

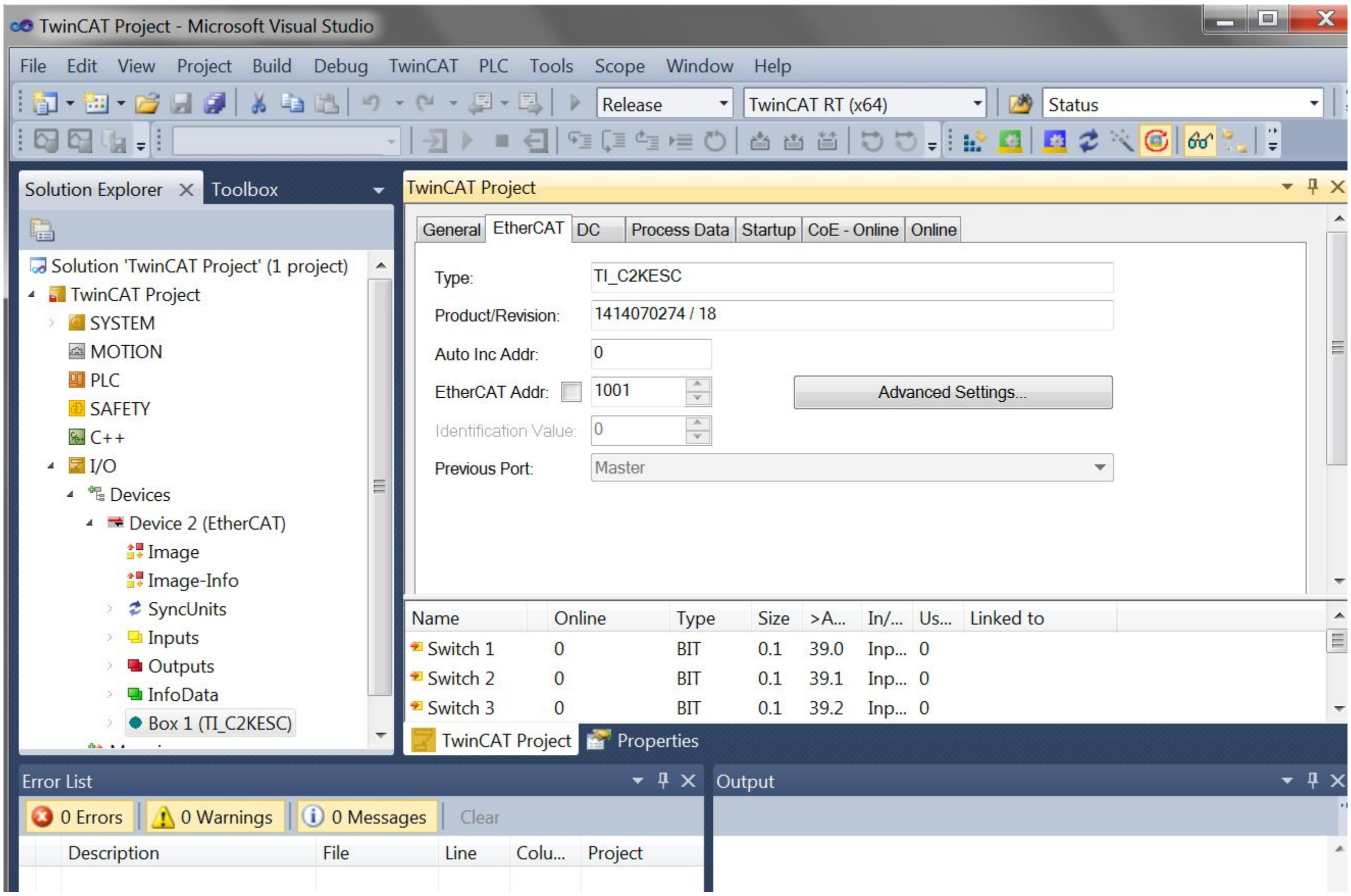

Figure 26. TwinCAT Project EtherCAT Tab

2. In the advanced settings popup windows, select “Smart View” to bring up detailed information about the EtherCAT Slave PDI. Click “Write E2PROM”. Note that, prior to initialization, this view shows a “blank” configuration.

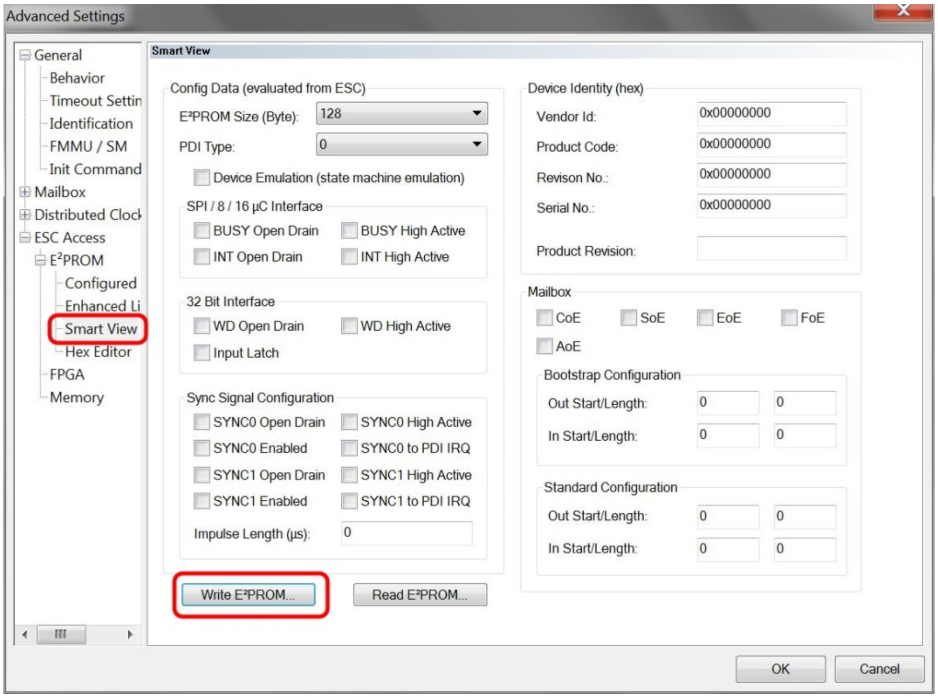

Figure 27. TwinCAT "Smart View" Slave Properties Window Showing Blank Slave

3. Click “Browse” to find the desired EEPROM binary associated with either the SPI or EMIF interface in the TMDSECATCNCD379D_PDI_HAL_API directory downloaded from the project site.
   (a) pdi_test_app_spi.bin – for SPI interface
   (b) pdi_test_app_emif.bin – for EMIF interface
   (c) Click “OK”.

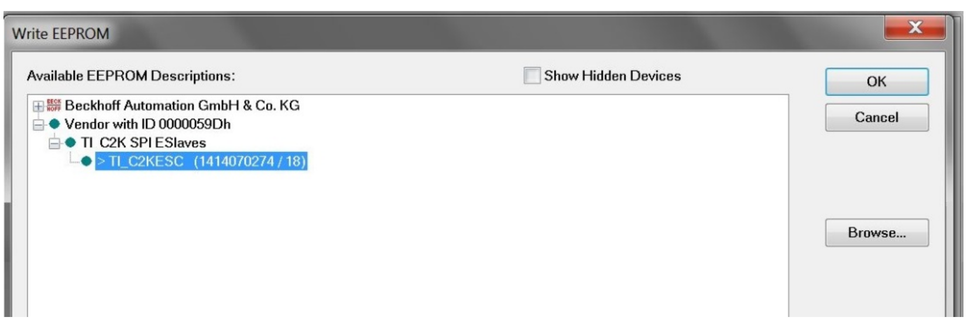

Figure 28. TwinCAT3 EEPROM File Dialog

4. After TwinCAT writes the EEPROM (in this case for the SPI), the following “Smart View” window showing a valid configuration with PDI Type = “SPI slave” should appear (see Figure 29).

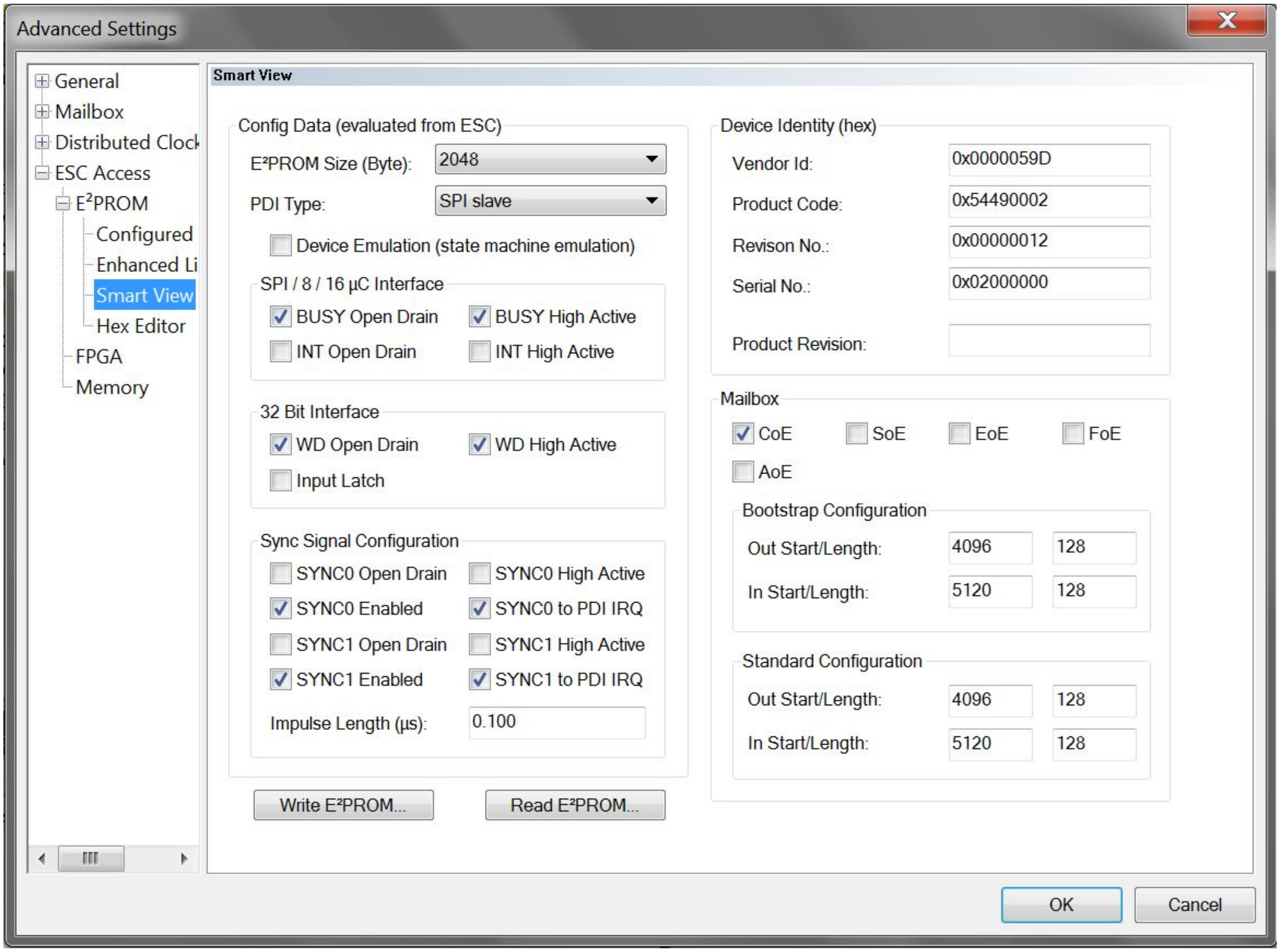

Figure 29. TwinCat "Smart View" Slave Properties Window Showing Programmed EEPROM

5. The EtherCAT Slave controller is now prepared for communication with the MCU.

3.5 EEPROM Configuration Values

The first 15 bytes of the EEPROM hold MCU-related configuration. This is readable via several ESC register addresses. The options used in these demonstrations are:

Table 3. EEPROM MCU Configuration

ESC Register Address[Bit]	Value	Description
Common Settings		
0x140	0x05 – SPI 0x08 – EMIF	PDI type
0x141[0]	Off	Device emulation
0x141[1]	All Ports On	Enhanced Link Detection
0x141[3:2]	DC Latch + Sync Unit	DC Units power saving
ASYNC16 Settings		
0x150[1:0]	Push-pull active high	BUSY output driver/polarity
0x150[3:2]	Push-pull active low	IRQ output driver/polarity
0x150[4]	Active low	BHE polarity
0x150[7]	Active low	RD polarity
0x152[0]	Normal delay	Read BUSY delay
0x151[2]	LATCH input	SYNC0/LATCH0
0x151[3]	On	Map to AL Event Request
0x151[6]	LATCH input	SYNC1/LATCH1
0x151[7]	On	Map to AL Event Request
SPI Settings		
0x150[1:0]	Mode 3	SPI mode
0x150[3:2]	Push-pull active low	SPI_IRQ output driver/polarity
0x150[4]	Active low	SPI_SEL polarity
0x150[5]	Normal sample	Data Out sample mode
0x151[1:0]	Push-pull active low	Output driver/polarity
0x151[2]	SYNC output	SYNC0/LATCH0
0x151[3]	On	Map to AL Event Request
0x151[5:4]	Push-pull active low	Output driver/polarity
0x151[6]	SYNC output	SYNC1/LATCH1
0x151[7]	On	Map to AL Event Request

4 Getting Started (Firmware)

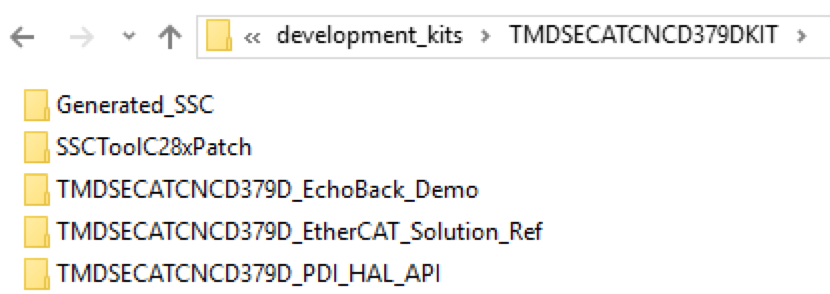

Figure 30. TMDSECATCNCD379DKIT controlSUITE Folders

The firmware package for this kit consists of a Process Data Interface (PDI) demo using the hardware abstraction layer (HAL), C2000 patches for the Beckhoff slave stack code (SSC), a reference project for the SSC, and a precompiled echo-back demo that uses the patched SSC. All of this software is designed for C2000 F2837x MCUs. Each demo has build configurations for SPI and EMIF. To change between these interfaces, set both of the switches in switch block SW1 (Figure 25) on the adapter board accordingly.

The PDI demo sets up and tests basic communication between the EtherCAT master and the EtherCAT slave controller. The echo-back demo shows an example of higher-level communication between the master and slave.

NOTE: For EtherCat Developers: The EtherCAT Technology Group (ETG) recommends membership for parties implementing EtherCAT in a machine or machine line. For additional information about EtherCAT and ETG membership, see the following links:

- EtherCAT FAQs: https://www.ethercat.org/en/faq.html
- EtherCAT Technology Group site: https://www.ethercat.org

4.1 PDI HAL Test Demo

The PDI test application contains a hardware abstraction layer (HAL) that handles all of the configuration details for the EMIF or SPI interface. This Code Composer Studio™ (CCS) 7.x project also performs some simple read/write tests to verify correct functioning of communication with the ET1100 slave controller.

The CCS project files for pdi_hal_test_app can be downloaded from the design directory at http://www.ti.com/tool/TMDSECATCNCD379D. The files install into the C:\TI\controlSUITE\development_kits\TMDSECATCNCD379DKIT directory. Once downloaded, import this project into CCS 7.0 or later using the procedure below:

1. File → Import… (an “Import” popup window appears).
2. Select “Code Composer Studio” → CCS Projects. Click “Next”.
3. Use “Select search-directory” and click “Browse” to find the pdi_hal_test_app source directory.
4. Select pdi_hal_test_app from the list of Discovered projects:
   (a) Leave the “Automatically import referenced projects” box checked.
   (b) Checking the box for “Copy projects into workspace” is optional.
   (c) Click “Finish”. The CCS project will appear in the project explorer window.

4.1.1 Test Setup

The main purpose of this test is to demonstrate the usage of the PDI between the C28x processor and the ET1100 EtherCAT Slave Controller.

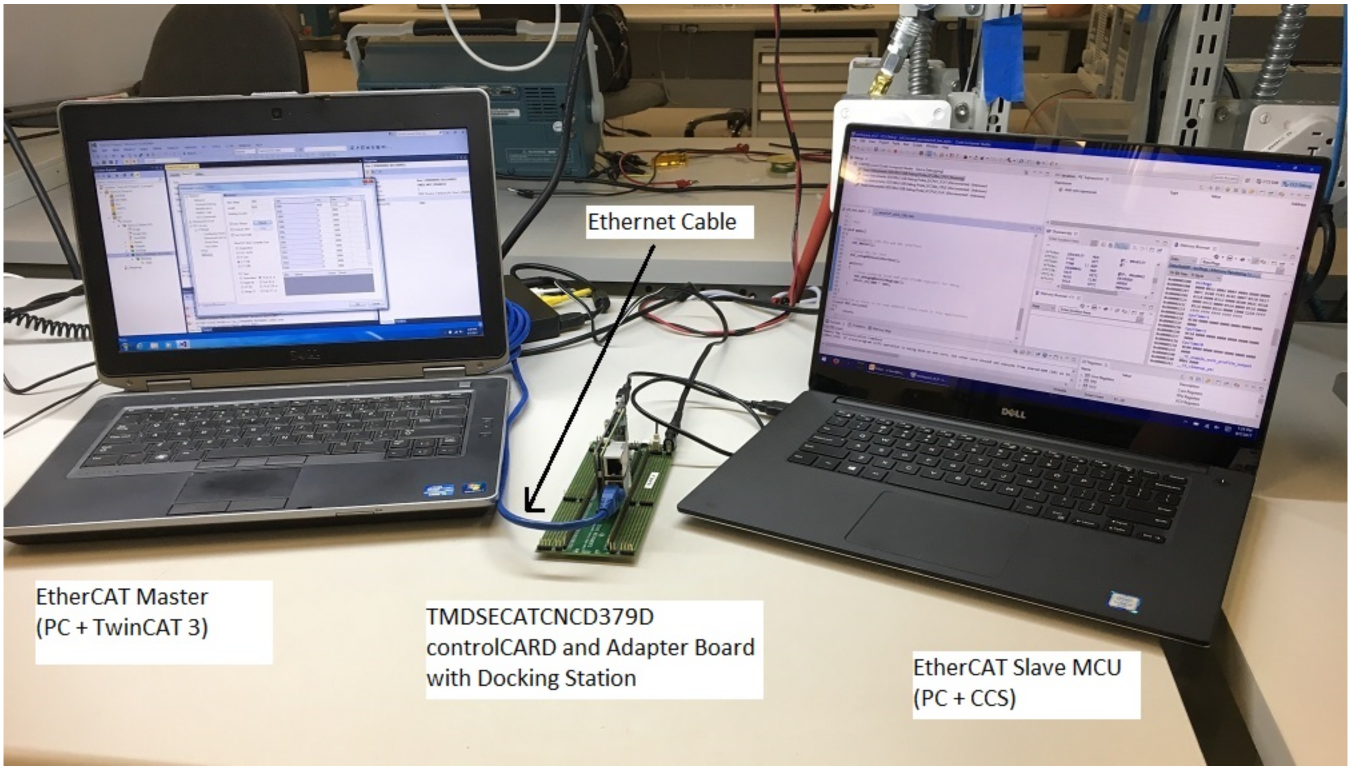

Figure 31. EtherCAT Test Setup

The test setup in Figure 31 shows a C2000 F28379D controlCARD with attached EtherCAT adapter board and two PCs. The left PC connects to the adapter board through a standard Ethernet cable connected to Port 0, and runs TwinCAT 3 software, which provides EtherCAT Master functionality. The right PC connects to the controlCARD directly through the USB connector and runs the EtherCAT Hardware abstraction layer (HAL) software on the CCS 7.x development environment. The HAL software in this example performs the following functions:

- Initialize the C28x hardware and the selected PDI interface (SPI or EMIF)
- Execute reads/writes to the ET1100 User RAM
- Execute reads from ET1100 register space

The intent of this project is to demonstrate the usage of the PDI. Therefore, no EtherCAT stack is included in this demo.

Note that the HAL software supports both the SPI and EMIF as PDI interfaces. The user must choose the proper settings when building the project. Correct jumper settings on the adapter board are also required for proper operation. These settings are described in Section 3.3.

4.1.1.1 Running Simple ESC Interface Test on C28x

After downloading the software from the project directory at http://www.ti.com/tool/TIDM-DELFINO-ETHERCAT and importing the project into CCS, perform the following steps to exercise the PDI HAL:

1. Open the example project pdi_hal_test_app in CCS. The file pdi_test_appl.c has the main routine. The following code is of interest:

ESC_HWInit()	Initializes the C28x MCU and the PDI
ESC_setupPDITestInterface()	Set-up PDI interface and initialize test variables and ET1100 RAM over PDI
ESC_debugUpdateESCRegLogs()	Keep updating ET1100 registers in a loop. User can add to the list of registers to read in the escRegs data structure.

```
void main()
{
    //Initialize C28x MCU and HAL interface
    ESC_HWInit();

    //setup PDI for test
    ESC_setupPDITestInterface();

    while(1)
    {
        //Keep updating local RAM with ET1100 registers for debug
        ESC_debugUpdateESCRegLogs();
        DELAY_US(1000 * 500);
    }

}
```

Figure 32. CCS Example Project: pdi_hal_test_app

2. Right click on the project and set the desired active build configuration. Figure 33 shows the available configurations, which provides options for program storage (flash and RAM) and interface type (EMIF, SPI-C):

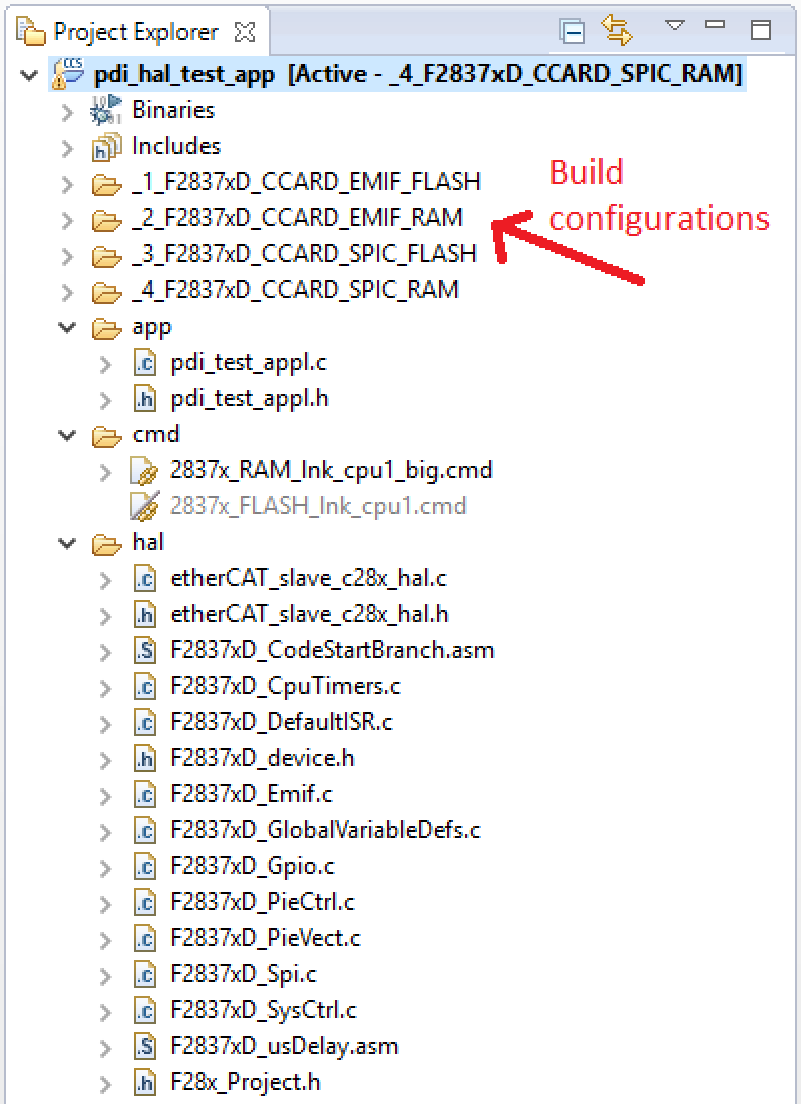

Figure 33. EtherCAT HW Abstraction Layer Project

For this example, choose build configuration (4_F2837xD_CCARD_SPIC_RAM) by right clicking on the project name and selecting “Build Configuration” → Set Active → (4_F2837xD_CCARD_SPIC_RAM).

Start TwinCAT3 on the EtherCAT Master PC as described in Section 3.2. Note that double clicking the EtherCAT slave node (“Box 2” in Figure 34) opens up a properties windows, from which the “Advanced Settings window” can be opened. This is used later in the demo.

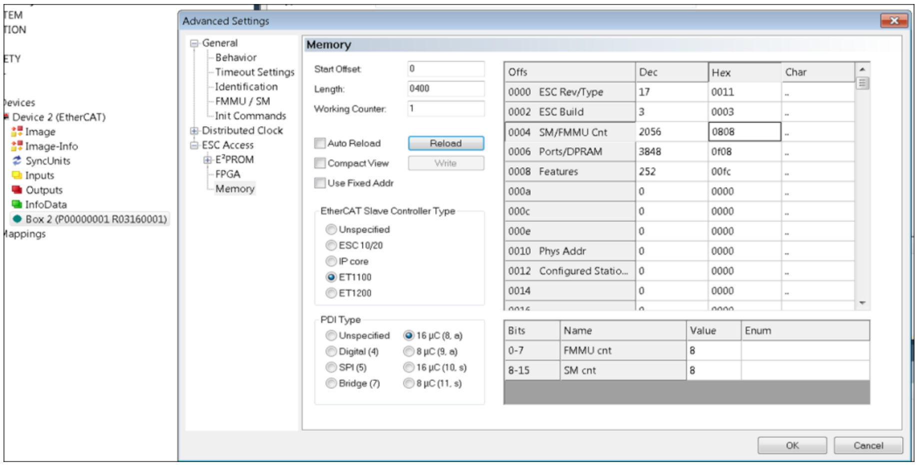

Figure 34. TwinCAT3 Advanced Settings Dialog

3. Start the debugger and open the memory browser window as shown in Figure 35. The “escRegs” data array contains a list of ET1100 register addresses and values. These get updated in the *ESC_debugUpdateESCRegLogs()* function.

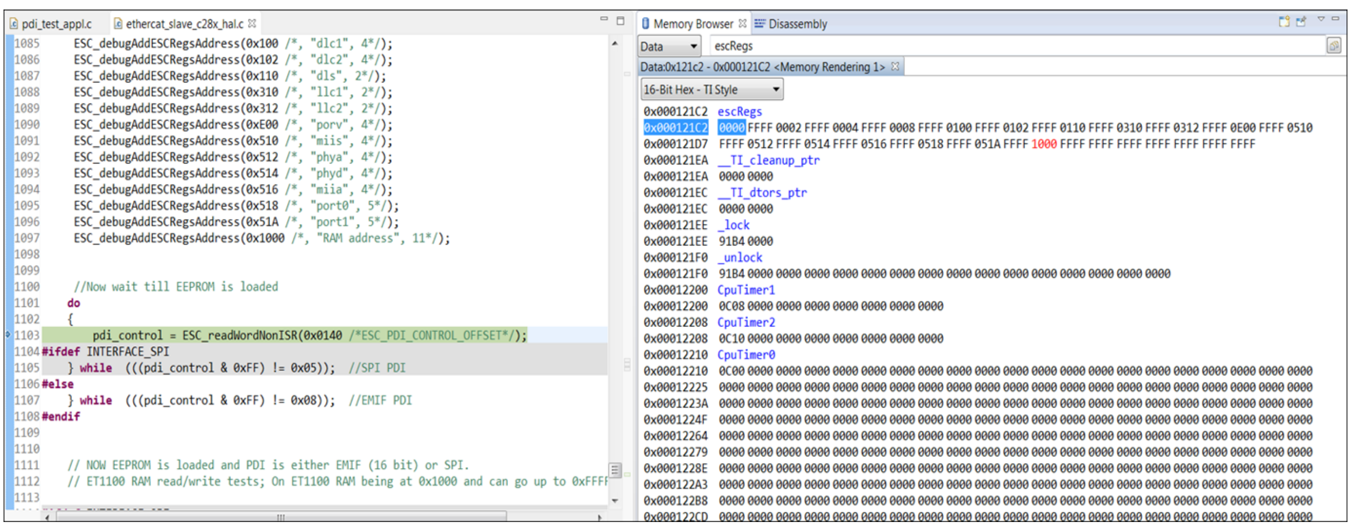

Figure 35. Device Debug Memory Window at INIT Time

NOTE: The ESC RUN LED will NOT be on during the memory tests, which is described in the following sections. For more information, see the ET1100 data sheet.

ESC RAM READ TEST

4. Open up the “advanced settings” window in TwinCAT3 and go to the memory browser at ESC Access → Memory and view Start Offset = 1000h as shown in Figure 36.

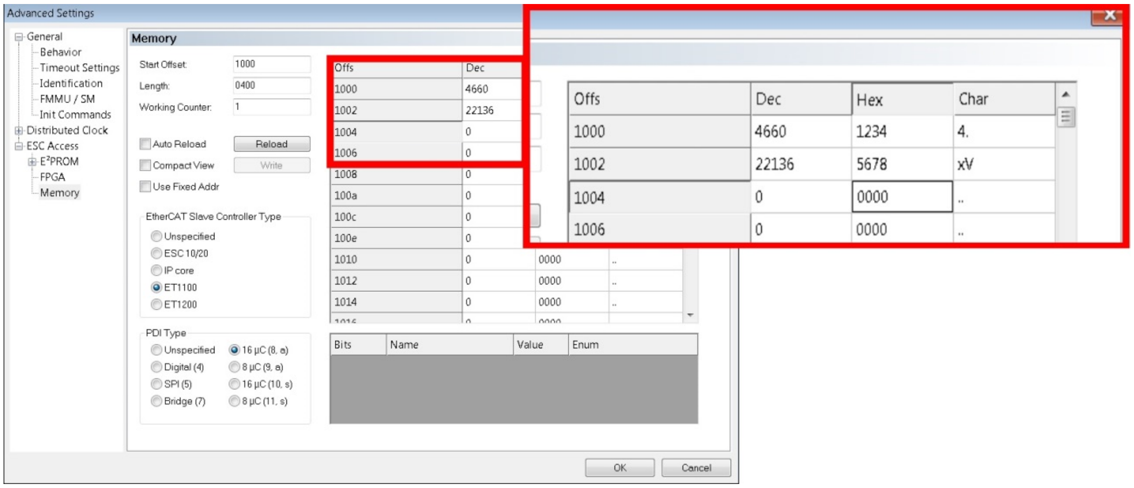

Figure 36. TwinCAT3 Memory Read Window

5. In CCS, view the Expressions window and add “escRegs” as a watched expression. Note that, as data is entered into the window in TwinCAT, the values read on the CCS side are identical.

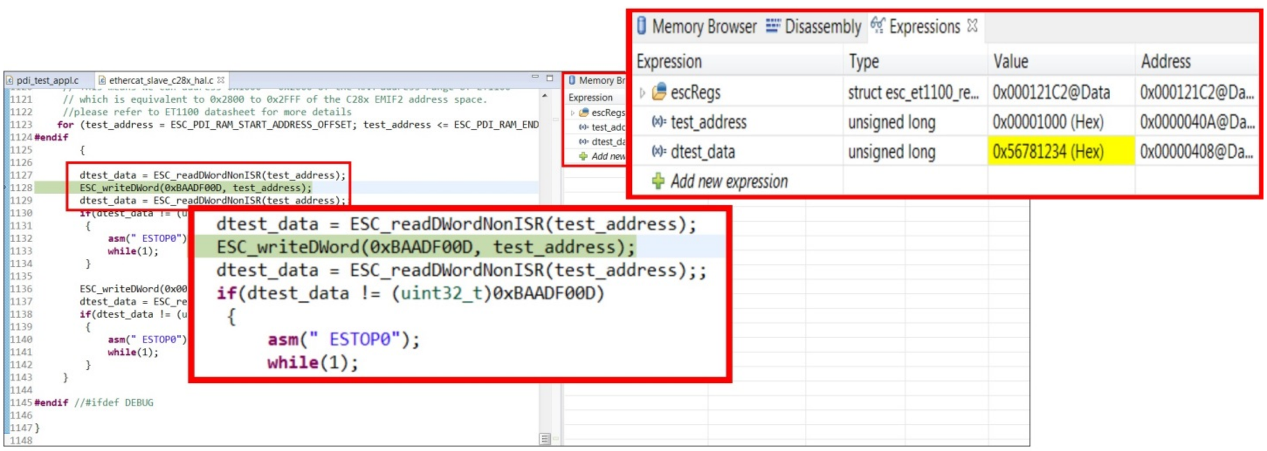

Figure 37. EtherCAT Write to Memory From CCS Project

ESC RAM WRITE TEST

6. Figure 38 shows program control after execution of the first 32-bit write and 32-bit read from PDI to ET100 address 0x1000.

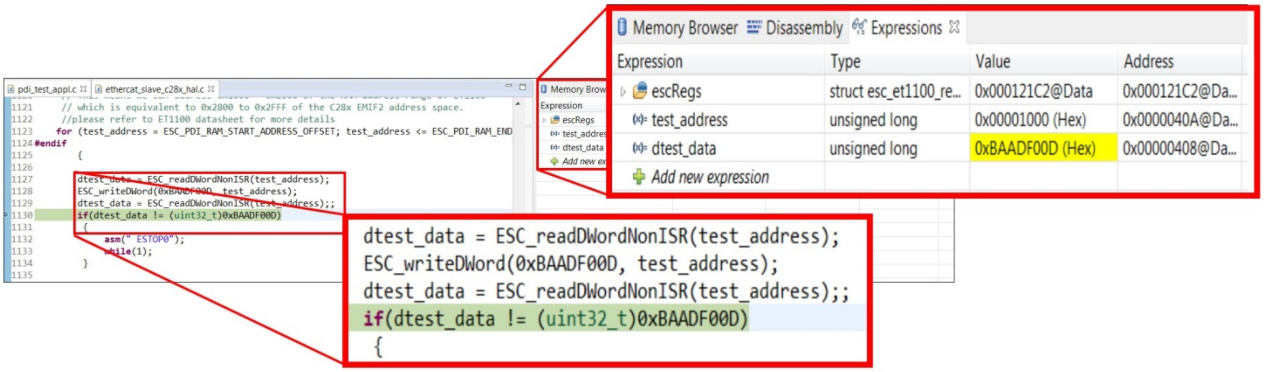

Figure 38. CCS Project Write to EtherCAT Slave

7. The TwinCAT Master view of the ESC memory address showing the results of the write from CCS.

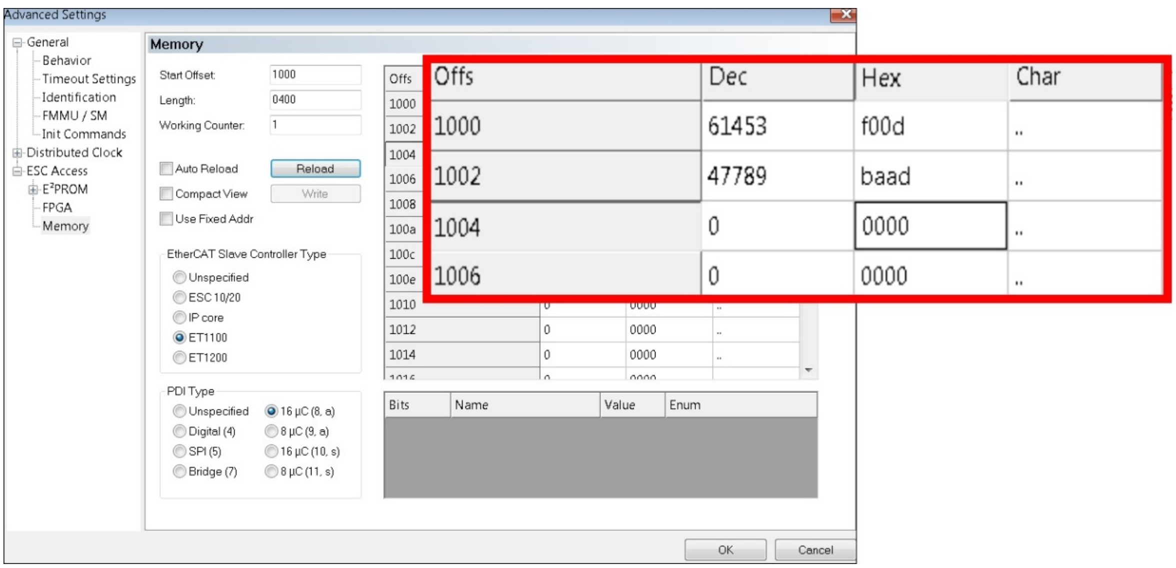

Figure 39. TwinCAT3 Master Read of Data Written to EtherCAT Slave

4.1.1.2 TwinCAT3 Troubleshooting

Common issues in TwinCAT3 usage:

- Problem: EtherCAT network fails to initialize
  - Other Descriptions: “Reload Devices” fails, “Scan” for devices fails, “Restart EtherCAT in config mode” fails.
- Solutions:
  - Power-cycle the controlCARD
  - Check to make sure a RealTime Ethernet Driver is available.
    TwinCAT → “Show RealTime Ethernet Compatible Devices”. This opens a popup window below.
    - Look for the first line “Installed and ready to use devices (realtime capable)”.

      In this example, there are NO adapters installed!
    - Select a compatible device; here it is “Local Area Connection → Intel ….” and click “Install”.
    - Close the window by clicking “X” in the upper right corner.

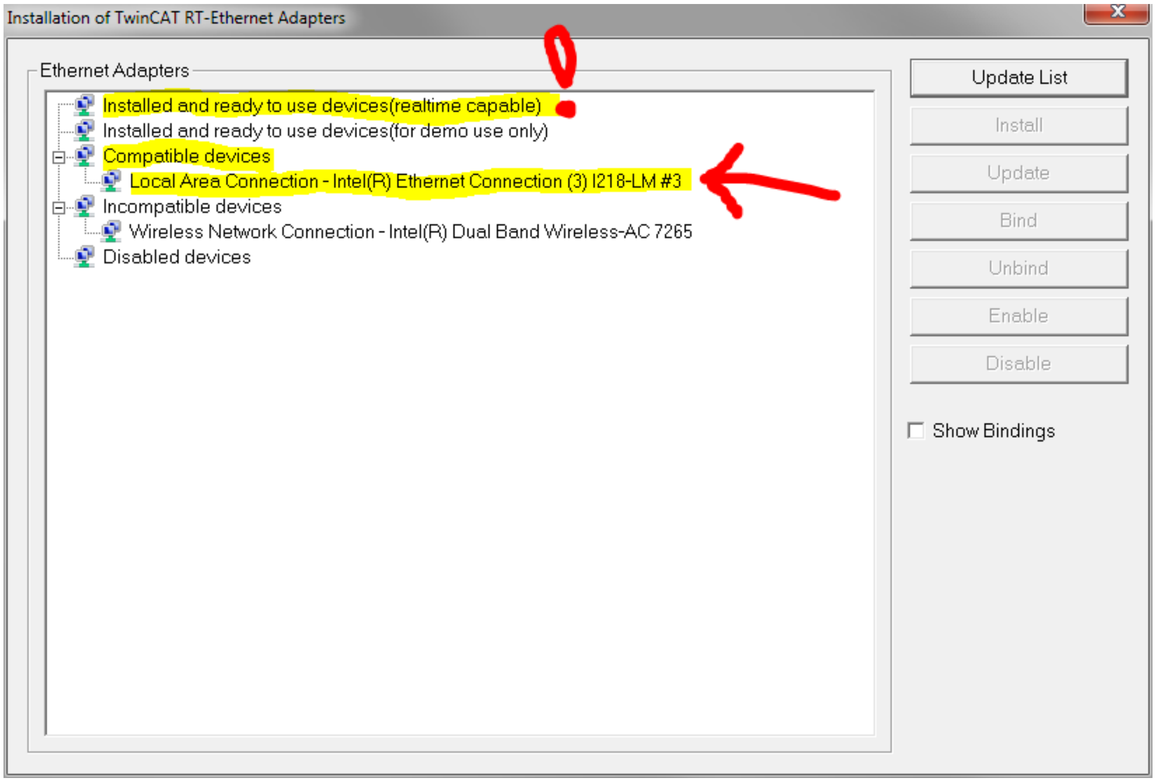

Figure 40. TwinCAT3 Ethernet Adapter Installation

4.1.2 Other Interfaces

It is possible to use EMIF1, SPI-A, or SPI-B to communicate with the ET1100, although the F28379D controlCARD and adapter board hardware do not support this directly. This functionality is implemented in the software and can be used on a custom board.

To use EMIF1, select one of the EMIF build configurations (_1_F2837xD_CCARD_EMIF_FLASH or _2_F2837xD_CCARD_EMIF_RAM). Uncomment the #define for USE_EMIF1 on line 526 of etherCAT_slave_c28x_hal.h:

```
525
526 //#define USE_EMIF1      //LAUNCHXL Rev2.0 J9 connector option for accessing ET1100
527                Uncomment
528 #ifdef CONTROLCARD  //for Controlcard definitions
529
530     #ifdef INTERFACE_SPI
531 #ifdef USE_EMIF1
532     #error "user cannot use EMIF1 with SPI Configurations of project"
533 #endif
534         extern void     ESC_SPIInit(void);
535         extern void ESC_SPIRead(uint16_t offset_addr,uint16_t numbytes, uint16_t* buffer);
536         extern void ESC_SPIWrite(uint16_t offset_addr,uint16_t *wrdata, uint16_t numwords) ;
537
538         #define ESC_SPI_INT_GPIO            136
539
540         //on ET1100 it is 8KB of RAM
541         #define ESC_PDI_RAM_START_ADDRESS_OFFSET    0x1000
542         #define ESC_PDI_RAM_END_ADDRESS_OFFSET      0x2FFF
543
544         #define ESC_SYNC0_GPIO              113
545         #define ESC_SYNC1_GPIO              114
546         #define ESC_RESET_ET1100_GPIO       137
547         #define ESC_EEPROM_LOADED_GPIO      119
548
549     #else //#ifdef INTERFACE_SPI
550
551         extern void setup_emif1_pinmux_async_16bit(Uint16 cpu_sel);
552         extern void ESC_EMIF2SetupPinmuxAsync16Bit(Uint16 cpu_sel);
553         extern void ESC_EMIF2WriteBlock(uint16_t* pData, uint16_t offset_addr,uint16_t numwords);
554
555         #ifdef USE_EMIF1 //LaunchPAD XL EMIF1 J9 connector option
556             //on ET1100 it is 8KB of RAM
557             #define ESC_PDI_RAM_START_ADDRESS_OFFSET    0x1000
558             #define ESC_PDI_RAM_END_ADDRESS_OFFSET      0x2FFF
559             #define ESC_EMIF_INT_GPIO                   107
560             #define ESC_SYNC0_GPIO                      86
561             #define ESC_SYNC1_GPIO                      87
562             #define ESC_RESET_ET1100_GPIO               108
563             #define ESC_EEPROM_LOADED_GPIO              52  //this was 33 on LAUNCXL Rev1.1
564
565         #else // #ifdef ESC_USE_EMIF1   //USE EMIF2
```

Figure 41. Code Change for Using EMIF1

To use another SPI module, select one of the SPI build configurations (_3_F2837xD_CCARD_SPIC_FLASH or _4_F2837xD_CCARD_SPIC_RAM). Add USE_SPIA or USE_SPIB to the predefined symbols list in the project build options. Remove USE_SPIC from the list:

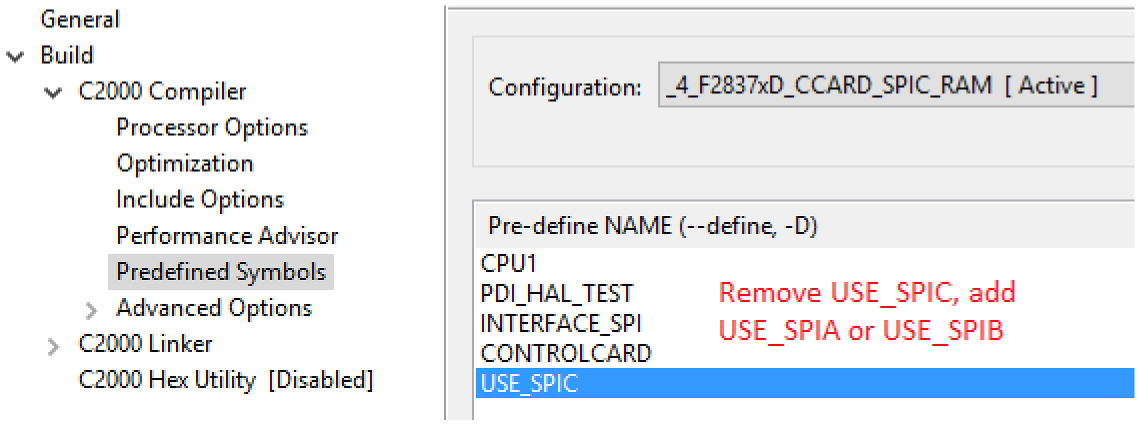

Figure 42. Project Configuration Change for Using SPI-A or SPI-B

This change affects the code in etherCAT_slave_c28x_hal.c:

```
//-------------------------------------------------------------------------
#ifdef INTERFACE_SPI
  //TxCnt=0;
  SPI_XmitInProgress=0;

  //InitSpiaGpio();
#ifdef USE_SPIA
  SpixRegs = &SpiaRegs;
  ESC_SPIAGpioInit();
#elif USE_SPIC
  SpixRegs = &SpicRegs;
  ESC_SPICGpioInit();
#else
  SpixRegs = &SpibRegs;
  ESC_SPIBGpioInit();
#endif
  ESC_SPIInitFIFO();
```

Define USE_SPIA or USE_SPIB in the project build options

Figure 43. SPI Selection and GPIO Configuration Code

4.2 EchoBack Demo

The EchoBack demo is a precompiled demonstration of the slave stack code. It emulates a bank of switches (inputs) and LEDs (outputs). The master controls the LEDs. The slave loops back the virtual LED signals into the virtual switches, so the master can read back the output state.

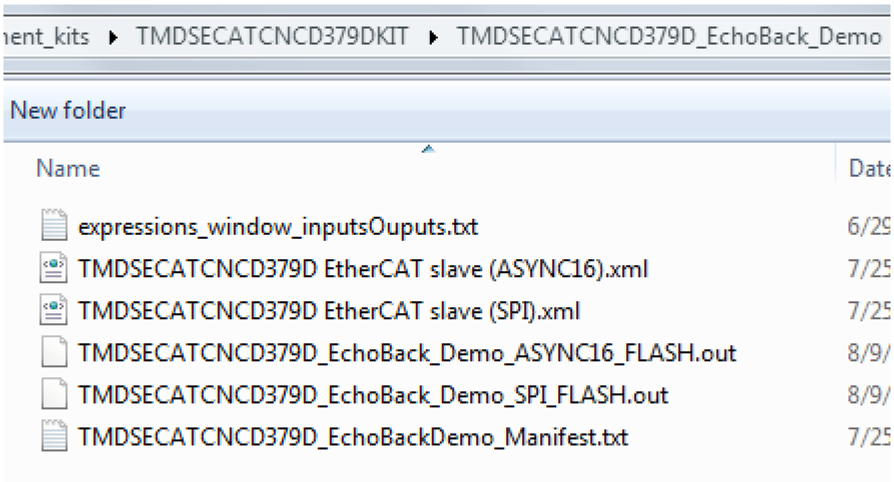

Figure 44. EchoBack Demo Files

4.2.1 Slave Setup

On the slave side, simply load the .out file for the chosen interface (ASYNC16 or SPI) using the CCS debugger. Run the program. To observe the variables, right-click in the Expressions window and choose Import. Select the expressions_window_inputsOutputs.txt file from the EchoBack demo directory, which is shown above.

4.2.2 Master Setup

The first step on the master side is to program the ET1100's EEPROM using TwinCAT. Unlike the PDI demo, this time the EEPROM is programmed using provided XML files, which can be seen in the directory listing above. Copy these XML files into the C:\TwinCAT\3.1\Config\Io\EtherCAT directory. Follow the same procedure as for the PDI demo (described in the Getting Started (Hardware) section of this document), but instead of clicking on Browse to select a binary EEPROM file, choose the appropriate TI option from the Available EEPROM Descriptions.

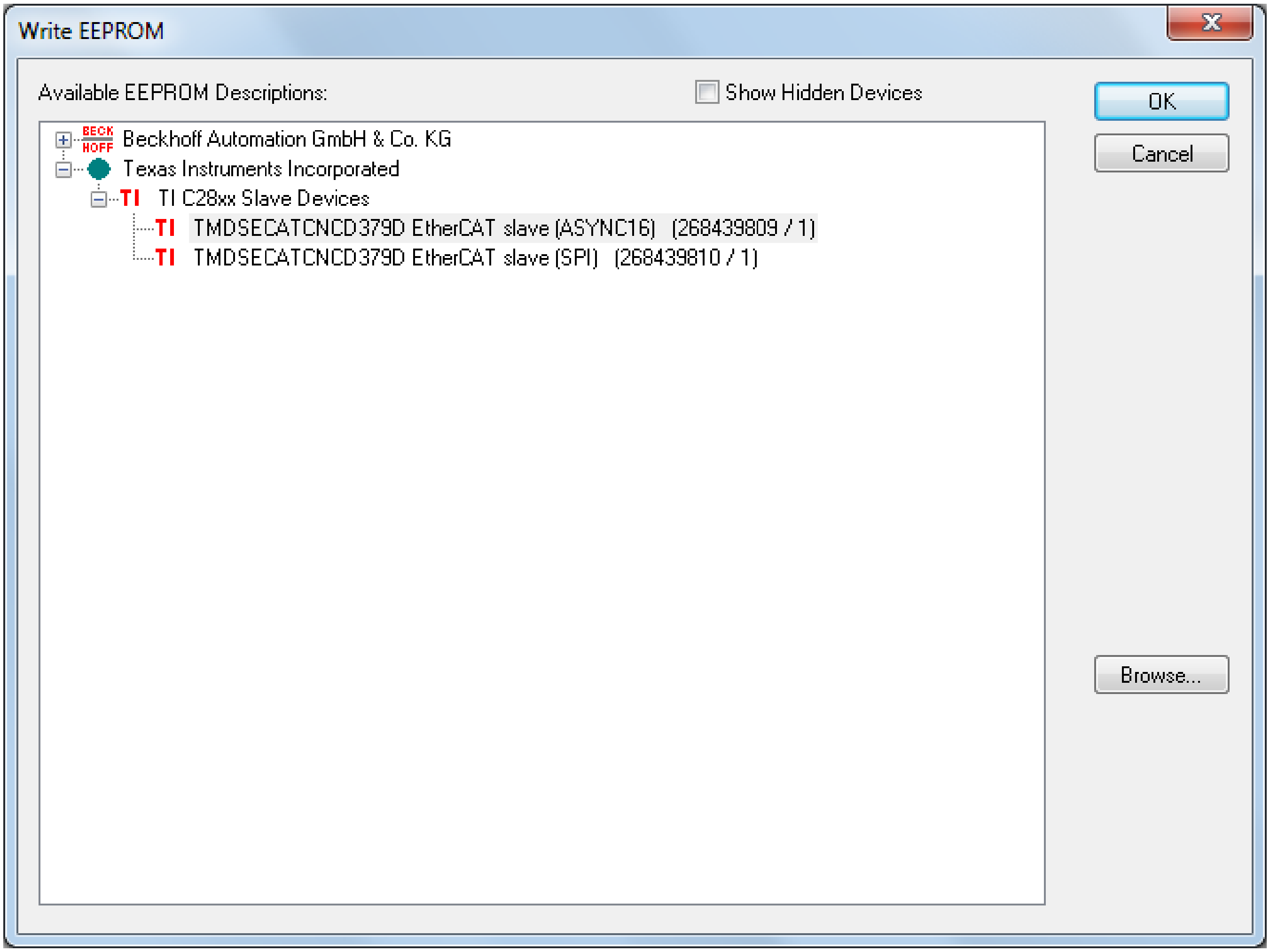

Figure 45. EchoBack EEPROM Configurations

Once the EEPROM is programmed, scan for devices again. If you've previously used another EtherCAT configuration such as the PDI demo, you will be prompted to overwrite the box description. To do so, click on Copy All, then OK.

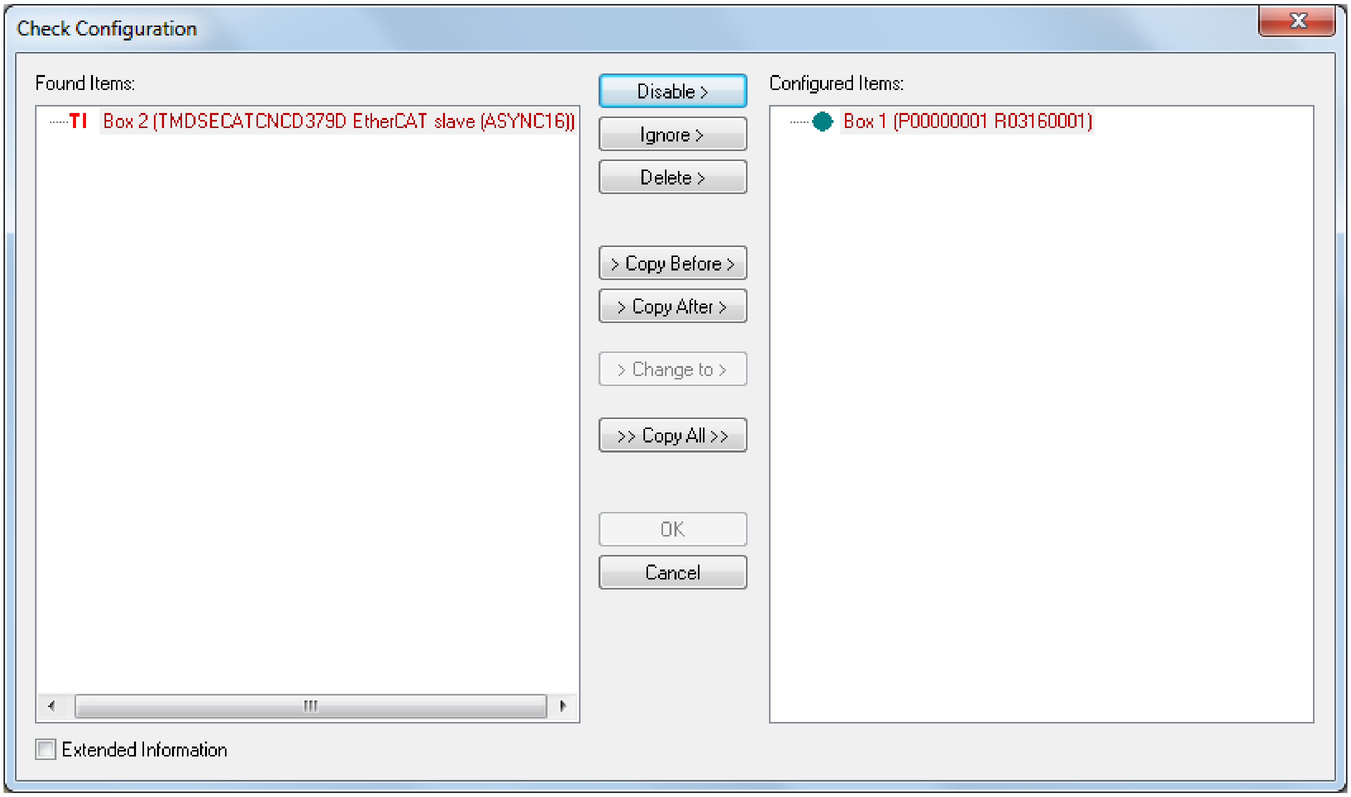

Figure 46. Overwriting Box Information

If the demo is running on the slave slide, a TwinCAT master can be used to toggle the LEDs and read the switch states. To toggle an LED, expand the box in the Solution Explorer pane. Click on "LEDs process data mapping" to see a list of the LEDs. Right-click on an LED and choose one of the Online Write options to set the LED value. The written value should appear immediately in the list.

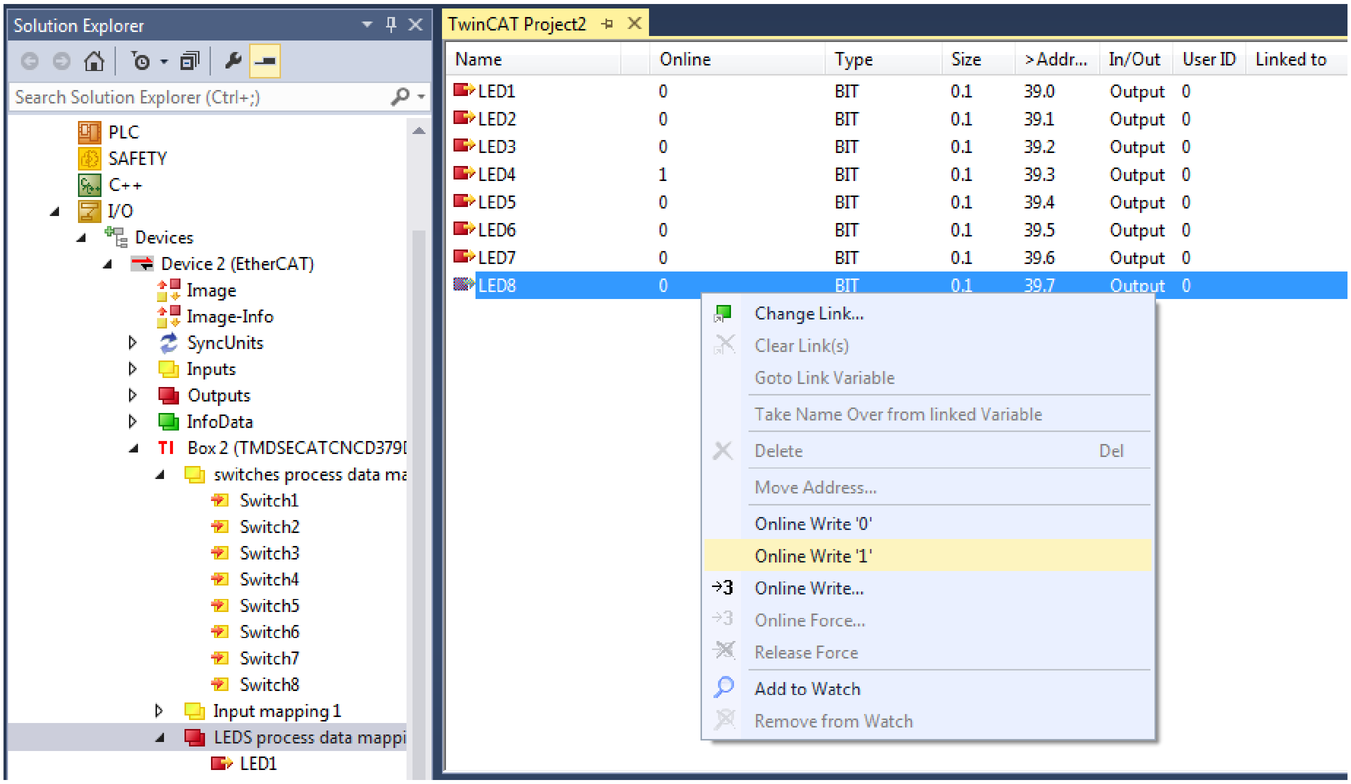

Figure 47. Writing to the LEDs

The LED values are looped back to the switches. The switches can be viewed by clicking on "switches process data mapping". Their values should match the LED values seen in "LEDs process data mapping".

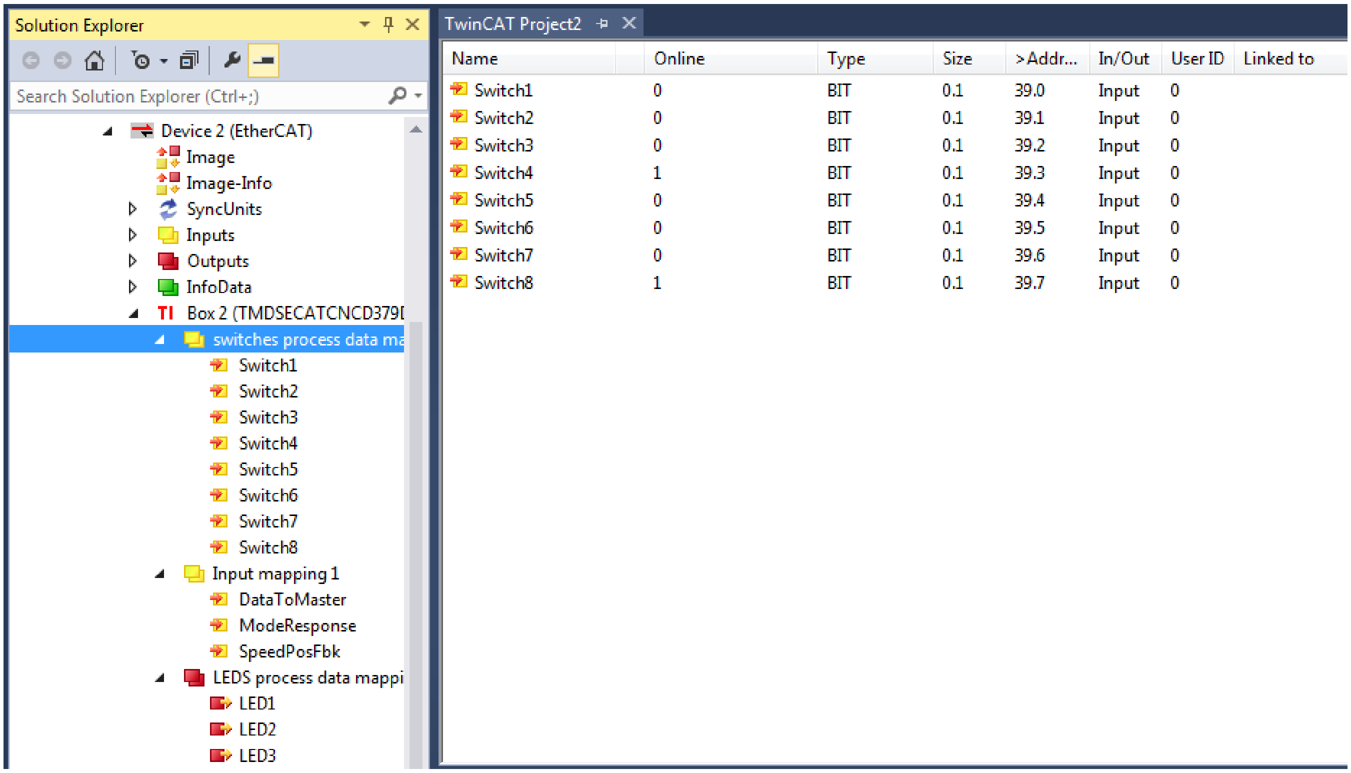

Figure 48. Reading the Switches

This shows that full loopback has been achieved. The master can both read from and write to the slave.

4.3 Slave Stack Code

For information on the slave stack code patches as well as build and debugging instructions, see the *TMDSECATCNCD379D EtherCAT Solution Reference Guide* (SPRUIG9).

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
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4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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