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Low Power, HDMI to Dual Output LVDS Display Bridge

SCOPE

This reference manual provides a detailed description of the ADV7613 functionality and features.

Full specifications on the ADV7613 are available in the product data sheet, available from Analog Devices, Inc. The data sheet must be consulted in conjunction with this reference manual when working with the ADV7613.

FUNCTIONAL BLOCK DIAGRAM

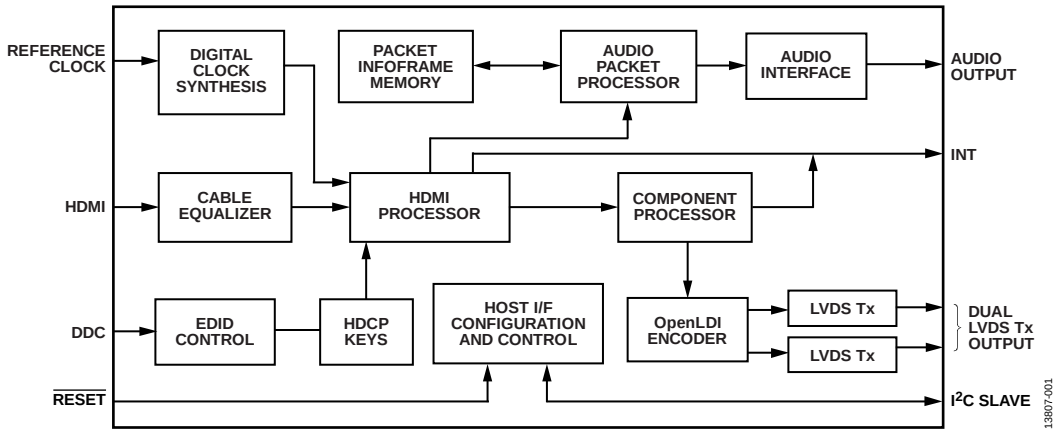

Figure 1. Functional Block Diagram

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REVISION HISTORY

6/2017—Rev. 0 to Rev. A

Changes to Figure 4 17
Changes to Introduction Section 161
Changes to LVDS Output Formatter Section, TX_PIXEL_SWAP, OpenLDI Tx, Address 0x4E[4] Section, Table 443, and Table 444 166

3/2016—Revision 0: Initial Version

USING THE ADV7613 REFERENCE MANUAL

NUMBER NOTATIONS

Table 1.

Notation	Description
Bit N	Bits are numbered in little endian format, that is, the least significant bit of a number is referred to as Bit 0.
V[x:y]	Bit field representation covering Bit x to Bit y of a value or a field (V).
0xNN	Hexadecimal (base 16) numbers are preceded by the prefix 0x.
0bNN	Binary (base 2) numbers are preceded by the prefix 0b.
NN	Decimal (base 10) are represented using no additional prefixes or suffixes.

FIELD FUNCTION DESCRIPTIONS

Throughout this reference manual, a series of function tables are provided. The function of a field is described in a table preceded by the bit name, a short function description, the I²C map, the register location within the I²C map, and a detailed description of the field.

The detailed description consists of the following:

- The values that can be read back from the field (for a readable field)
- The values that the field can be set to (for a writable field)

Example Field Function Description

The following is an example of a field function table followed by a description of each part of the table.

PRIM_MODE[3:0], IO Map, Address 0x01[3:0]

This register is a control for selecting the primary mode of operation of the device.

Table 2. PRIM_MODE Function Description

PRIM_MODE[3:0]	Description
0000	Reserved
0001	Reserved
0010	Reserved
0011	Reserved
0100	Reserved
0101	HDMI component
0110 (default)	HDMI graphics
0111 to 1111	Reserved

In this example, the name of the field is PRIM_MODE and it is four bits long. Address 0x01 is the I²C location of the field in big endian format (MSB first, LSB last). The address is followed by a detailed description of the field. The first column of the table lists values the field can take or can be set to. These values are in binary format if not preceded by 0x or in hexadecimal format if preceded by 0x. The second column describes the function of each field for each value the field can take or can be set to. Values are in binary format.

REFERENCES

CEA, CEA-861-D, A DTV Profile for Uncompressed High Speed Digital Interfaces, Revision D, July 18, 2006.

Digital Content Protection (DCP) LLC, High-Bandwidth Digital Content Protection System, Revision 1.4, July 8, 2009.

HDMI Licensing and LLC, High-Definition Multimedia Interface, Revision 1.4a, March 4, 2010.

ITU, ITU-R BT.656-4, Interface for Digital Component Video Signals in 525-Line and 625-Line Television Systems Operating at the 4:2:2 Level of Recommendation ITU-R BT.601, February 1998.

INTRODUCTION TO THE ADV7613

The ADV7613 is a high quality, low power, single-input, high-definition multimedia interface (HDMI) to LVDS display bridge.

The ADV7613 incorporates a single-input HDMI receiver that supports high definition television (HDTV) formats up to 1080p, 8 bits per channel.

The ADV7613 also integrates a consumer electronics control (CEC) controller that supports the capability discovery and control (CDC) feature.

Each HDMI port has dedicated 5 V detect and hot plug assert pins. The HDMI receiver also includes an integrated equalizer that ensures robust operation of the interface with long cables.

Fabricated in an advanced CMOS process, the ADV7613 is provided in a 9 mm × 9 mm, 100-ball CSP_BGA, RoHS-compliant package and is specified over the −40°C to +85°C temperature range.

HDMI RECEIVER

The HDMI receiver on the ADV7613 supports 2.25 Gbps data bandwidth. The ADV7613 HDMI receiver incorporates active equalization of the HDMI data signals to compensate for the losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. The equalizer is highly effective and is capable of equalizing for long cables to achieve robust receiver performance.

With the inclusion of HDCP, displays can receive encrypted video content. The HDMI interface of the ADV7613 allows a video receiver to authenticate, decrypt encoded data, and renew that authentication during transmission, as specified by the HDCP v1.4 protocol for both the active and background HDMI ports.

The ADV7613 offers a flexible audio output port for audio data extraction from the HDMI stream. HDMI audio formats, including super audio CD (SACD) via Direct Stream Digital® (DSD) and high bit rate (HBR), are supported by the ADV7613. The HDMI receiver has advanced audio functionality, such as a mute controller, which prevents audible extraneous noise in the audio output.

COMPONENT PROCESSOR

The ADV7613 contains a component processor (CP), which processes the video data up to 1080p. The CP section provides color adjustment features, such as brightness, saturation, and hue. The color space conversion (CSC) matrix allows the color space to be changed as required. The standard detection and identification (STDI) block allows the detection of video timings.

MAIN FEATURES OF THE ADV7613

HDMI Receiver

The HDMI receiver supports the following features:

- HDMI features supported
  - 148.5 MHz maximum transition minimized differential signaling (TMDS) clock frequency
  - Full colorimetry including sYCC601, Adobe RGB, Adobe YCC601, xvYCC extended gamut color
  - CEC 1.4 compatible
- HDCP 1.4 support
- Supports all display resolutions up to 1920 × 720 at 60 Hz, 8-bit
- Supports many audio formats including DSD, HBR, S/PDIF (IEC60958 compatible) with sampling frequency up to 192 kHz
- Programmable front-end equalization for long cable lengths
- Audio mute for removing extraneous noise
- Programmable interrupt generator to detect HDMI packets
- Internal extended display identification (EDID) support
- Repeater support, up to 127 key selection vectors (KSVs)

Component Video Processing

The ADV7613 supports the following component video processing features:

- An any-to-any 3 × 3 CSC matrix support YCrCb to RGB and RGB to YCrCb
- Provides color controls, such as saturation, brightness, hue, and contrast
- Standard detection and identification (STDI) block that enables format detection
- Free run output mode provides stable timing when no video input is present

Video Output Formats

The ADV7613 outputs the following LVDS video formats: VESA mapping and OpenLDI mapping.

FUNCTIONAL BLOCK DIAGRAM

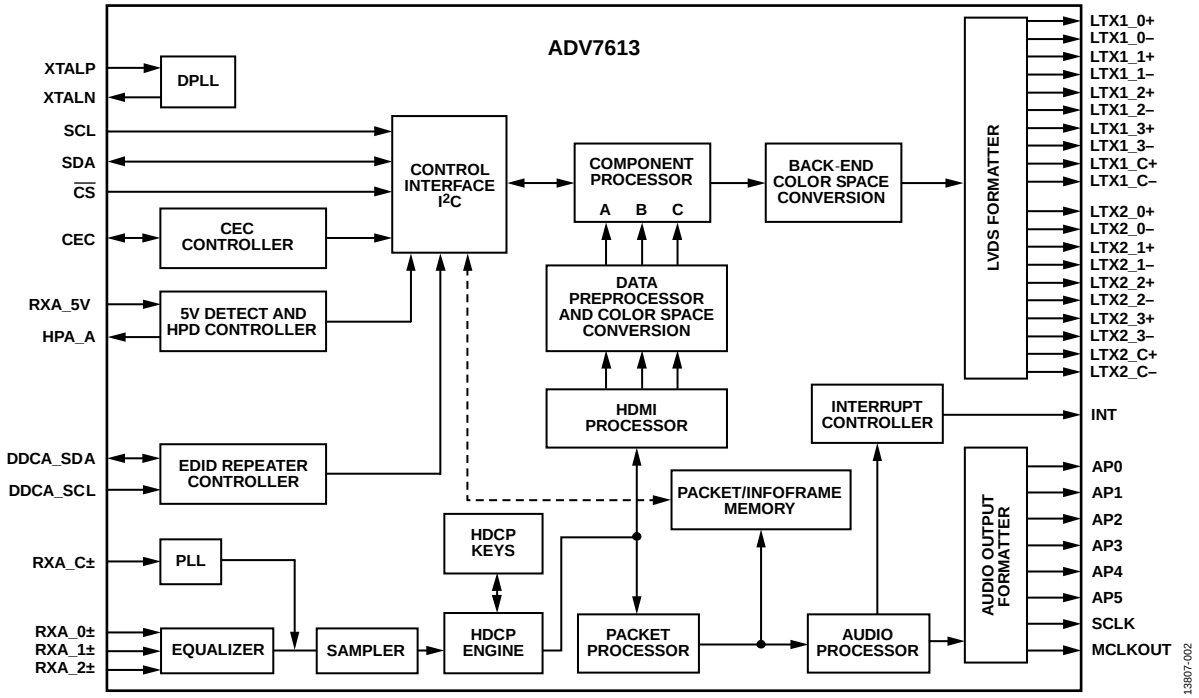


Figure 2. Detailed Functional Block Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

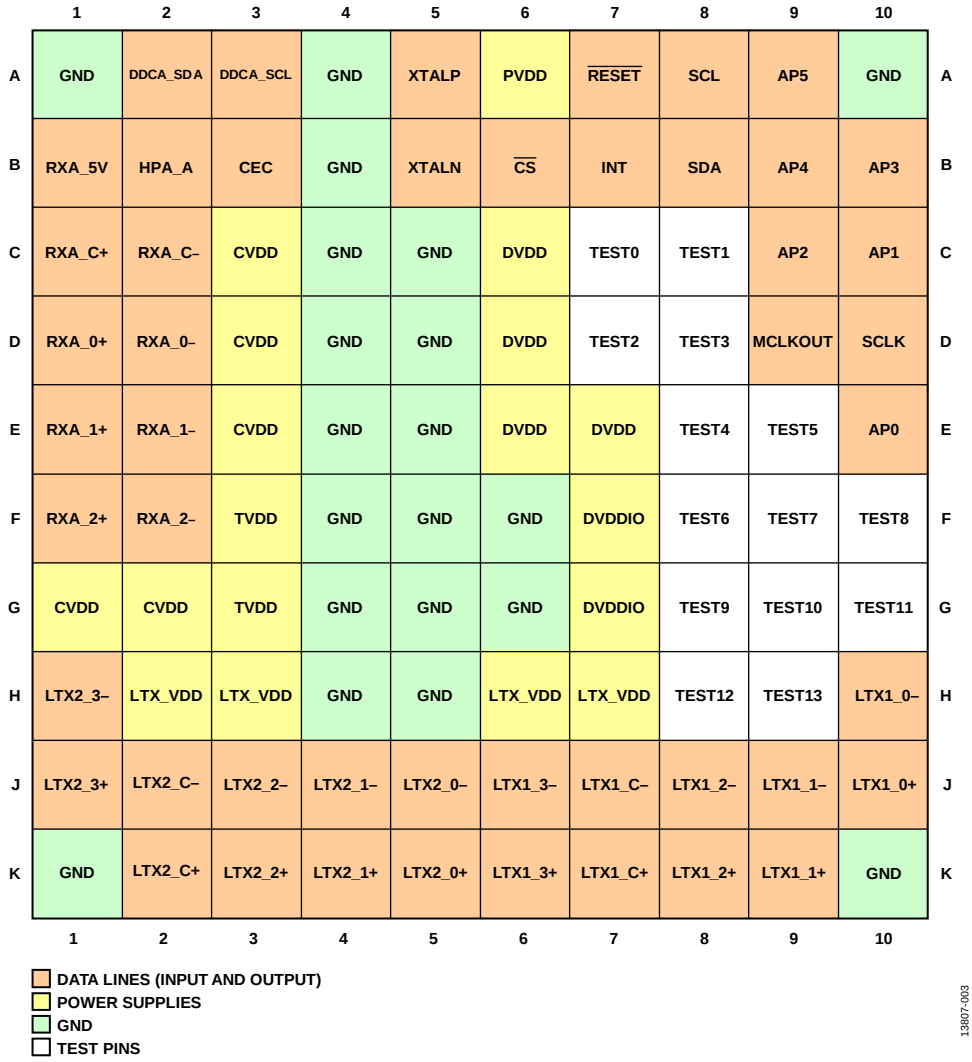


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No	Mnemonic	Type	Description
A1, A4, A10, B4, C4, C5, D4, D5, E4, E5, F4 to F6, G4 to G6, H4, H5, K1, K10	GND	Ground	Ground.
A2	DDCA_SDA	HDMI Rx DDC	HDCP Slave Serial Data for HDMI Port A.
A3	DDCA_SCL	HDMI Rx DDC	HDCP Slave Serial Clock for HDMI Port A.
A5	XTALP	Miscellaneous analog	Input for 28.63636 MHz Crystal or an External 1.8 V, 28.63636 MHz Clock Oscillator Source to Clock the ADV7613.
A6	PVDD	Power	Digital PLL Supply Voltage (1.8 V).
A7	$\overline{\text{RESET}}$	Miscellaneous digital	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7613 circuitry.
A8	SCL	Miscellaneous digital	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
A9	AP5	Audio output	Audio Output Pin 5. This pin is configurable to output S/PDIF digital audio, HBR or DSD. The AP5 pin typically provides the LRCLK signal for the I^2S modes.
B1	RXA_5V	HDMI input	5 V Detect Pin for HDMI Port A.
B2	HPA_A	Miscellaneous digital	Hot Plug Assert. This pin can be configured to output the hot plug assert signal for HDMI Port A.
B3	CEC	Digital input/output	Consumer Electronics Control Channel.

Pin No	Mnemonic	Type	Description
B5	XTALN	Miscellaneous analog	Crystal Output.
B6	$\overline{CS}$	Miscellaneous digital	Chip Select. This pin must be set low for the ADV7613 to process I²C messages. Pulling this line up causes the I²C state machine to ignore I²C transmission.
B7	INT	Miscellaneous digital	Interrupt. This pin can be active low or active high, open drain or transistor to transistor logic (TTL). The events that trigger an interrupt are under user configuration.
B8	SDA	Miscellaneous digital	I²C Port Serial Data Input/Output. SDA is the data line for the control port.
B9	AP4	Audio output	Audio Output 4. This pin is configurable to output S/PDIF digital audio, HBR, or I²S.
B10	AP3	Audio output	Audio Output 3. This pin is configurable to output S/PDIF digital audio, HBR, or I²S.
C1	RXA_C+	HDMI input	Digital Input Clock True of HDMI Port A.
C2	RXA_C−	HDMI input	Digital Input Clock Complement of HDMI Port A.
C3, D3, E3, G1, G2	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
C6, D6, E6, E7	DVDD	Power	Digital Core Supply Voltage (1.8 V).
C7, C8, D7, D8, E8, E9, F8 to F10, G8 to G10, H8, H9	TEST0 to TEST13	Miscellaneous	Test Pins. Connect these pins to ground via 1 kΩ resistors.
C9	AP2	Audio output	Audio Output 2. This pin is configurable to output S/PDIF digital audio, HBR, DSD, or I²S mode.
C10	AP1	Audio output	Audio Output 1. This pin is configurable to output S/PDIF digital audio, HBR, or DSD.
D1	RXA_0+	HDMI input	Digital Input Channel 0 True of HDMI Port A.
D2	RXA_0−	HDMI input	Digital Input Channel 0 Complement of HDMI Port A.
D9	MCLKOUT	Audio output	Master Clock. This pin is configurable to output the audio master clock signal.
D10	SCLK	Audio output	Serial Clock. This pin is configurable to output the audio serial clock.
E1	RXA_1+	HDMI input	Digital Input Channel 1 True of HDMI Port A.
E2	RXA_1−	HDMI input	Digital Input Channel 1 Complement HDMI Port A.
E10	AP0	Audio Output	Audio Output 0. This pin is configurable to output S/PDIF digital audio, HBR, DSD, or I²S.
F1	RXA_2+	HDMI input	Digital Input Channel 2 True of HDMI Port A.
F2	RXA_2−	HDMI input	Digital Input Channel 2 Complement of HDMI Port A.
F3, G3	TVDD	Power	Termination Supply Voltage (3.3 V).
F7, G7	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
H1	LTX2_3−	LVDS output	LVDS Output Channel 3 Complement of LVDS Output Port 2.
H2, H3, H6, H7	LTX_VDD	Power	LVDS Supply Voltage (1.8 V).
H10	LTX1_0−	LVDS output	LVDS Output Channel 0 Complement of LVDS Output Port 1.
J1	LTX2_3+	LVDS output	LVDS Output Channel 3 True of LVDS Output Port 2.
J2	LTX2_C−	LVDS output	LVDS Clock Complement of LVDS Output Port 2.
J3	LTX2_2−	LVDS output	LVDS Output Channel 2 Complement of LVDS Output Port 2.
J4	LTX2_1−	LVDS output	LVDS Output Channel 1 Complement of LVDS Output Port 2.
J5	LTX2_0−	LVDS output	LVDS Output Channel 0 Complement of LVDS Output Port 2.
J6	LTX1_3−	LVDS output	LVDS Output Channel 3 Complement of LVDS Output Port 1.
J7	LTX1_C−	LVDS output	LVDS Clock Complement of LVDS Output Port 1.
J8	LTX1_2−	LVDS output	LVDS Output Channel 2 Complement of LVDS Output Port 1.
J9	LTX1_1−	LVDS output	LVDS Output Channel 1 Complement of LVDS Output Port 1.
J10	LTX1_0+	LVDS output	LVDS Output Channel 0 True of LVDS Output Port 1.
K2	LTX2_C+	LVDS output	LVDS Clock True of LVDS Output Port 2.
K3	LTX2_2+	LVDS output	LVDS Output Channel 2 True of LVDS Output Port 2.
K4	LTX2_1+	LVDS output	LVDS Output Channel 1 True of LVDS Output Port 2.
K5	LTX2_0+	LVDS output	LVDS Output Channel 0 True of LVDS Output Port 2.
K6	LTX1_3+	LVDS output	LVDS Output Channel 3 True of LVDS Output Port 1.
K7	LTX1_C+	LVDS output	LVDS Clock True of LVDS Output Port 1.
K8	LTX1_2+	LVDS output	LVDS Output Channel 2 True of LVDS Output Port 1.
K9	LTX1_1+	LVDS output	LVDS Output Channel 1 True of LVDS Output Port 1.

GLOBAL CONTROL REGISTERS

The register control bits described in this section deal with the general control of the chip, and the CP and the HDMI receiver sections of the ADV7613.

ADV7613 REVISION IDENTIFICATION

RD_INFO[15:0], IO, Address 0xEA[7:0]; Address 0xEB[7:0] (Read Only)

This register contains the chip revision code.

Table 4. RD_INFO[15:0] Function Description

RD_INFO[15:0]	Description
0x20C4	ADV7613

POWER-DOWN CONTROLS

Primary Power-Down Controls

POWER_DOWN is the main power-down control. It is the main control for Power-Down Mode 0 and Power-Down Mode 1. See the Power-Down Modes section for more details.

POWER_DOWN, IO, Address 0x0C[5]

This register is the control that enables power-down mode. This is the main I²C power-down control.

Table 5. POWER_DOWN Function Description

POWER_DOWN	Description
0	Chip operational
1 (default)	Enables chip power down

Secondary Power-Down Controls

The following controls allow various sections of the ADV7613 to be powered down.

It is possible to stop the clock to the CP to reduce power for a power sensitive application. The CP_PWRDN bit enables this power save mode. The HDMI block is not affected by this power save mode. The CP_PWRDN bit allows the use of limited HDMI, STDI monitoring features while reducing the power consumption. For full processing of the HDMI input, the CP core must be powered up.

CP_PWRDN, IO, Address 0x0C[2]

This bit is the power-down control for the CP core.

Table 6. CP_PWRDN Function Description

CP_PWRDN	Description
0 (default)	Powers up clock to CP core.
1	Powers down clock to CP core. HDMI block not affected by this bit.

XTAL_PDN

XTAL_PDN allows the user to power down the crystal oscillator (XTAL) clock in the following sections:

- STDI blocks
- Free run synchronization generation block
- I²C sequencer block, which is used for the configuration of the gain, clamp, and offset
- CP and HDMI section

The XTAL clock is also provided to the HDCP engine, EDID, and the repeater controller within the HDMI receiver. The XTAL clock within these sections is not affected by XTAL_PDN.

XTAL_PDN, IO, Address 0x0B[0]

This bit is the power-down control for the XTAL in the digital blocks.

Table 7. XTAL_PDN Function Description

XTAL_PDN	Description
0 (default)	Powers up XTAL buffer to digital core
1	Powers down XTAL buffer to digital core

CORE_PDN

CORE_PDN allows the user to power down clocks, with the exception of the XTAL clock, in the following sections:

- CP block
- Digital section of the HDMI block

CORE_PDN, IO, Address 0x0B[1]

A power-down control for the data preprocessor (DPP), component processor (CP) core, and digital sections of the HDMI core.

Table 8. CORE_PDN Function Description

CORE_PDN	Description
0 (default)	Powers up CP and digital sections of HDMI block
1	Powers down CP and digital section of HDMI block

Power-Down Modes

The ADV7613 supports the following power-down modes:

- Power-Down Mode 0
- Power-Down Mode 1

Table 9 shows the power-down and normal modes of ADV7613.

Table 9. Power-Down Modes

POWER_DOWN Bit	CEC_POWER_UP Bit	CEC	EDID	Power-Down Mode
1	0	Disabled	Enabled	Power-Down Mode 0
1	1	Enabled	Enabled	Power-Down Mode 1
0	0	Disabled	Enabled[1]	Normal mode
0	1	Enabled	Enabled[1]	Normal mode

[1] Dependent on the values of EDID_A_ENABLE_CPU and EDID_A_ENABLE for the HDMI port.

Power-Down Mode 0

In Power-Down Mode 0, selected sections and pads are kept active to provide EDID and 5 V antiglitch filter functionality.

In Power-Down Mode 0, the sections of the ADV7613 are disabled except for the following blocks:

- I^2C slave section
- EDID/repeater controller
- EDID ring oscillator

The ring oscillator provides a clock to the EDID/repeater controller (refer to the E-EDID/Repeater Controller section) and the 5 V power supply antiglitch filter. The clock output from the ring oscillator runs at approximately 50 MHz.

The following pads only are enabled in Power-Down Mode 0:

- I^2C pads: SDA, SCL
- 5 V pads: RXA_5V, HPA_A
- DDC pads: DDCA_SCL, DDCA_SDA
- Reset pad: $\overline{\text{RESET}}$

Power-Down Mode 0 is initiated through a software (I^2C register) configuration.

Entering Power-Down Mode 0 via Software

The ADV7613 can be put into Power-Down Mode 0 by setting POWER_DOWN to 1 (default value) and CEC_POWER_UP to 0. This method allows an external processor to put the system in which the ADV7613 is integrated into standby mode. In this case, the CP and HDMI cores of the ADV7613 are kept powered up from the main power (for example, ac power) and set in or out of Power-Down Mode 0 through the POWER_DOWN bit.

Power-Down Mode 1

Power-Down Mode 1 is enabled when the following conditions are met:

- POWER_DOWN bit is set to 1
- CEC section is enabled by setting CEC_POWER_UP to 1

Power-Down Mode 1 provides the same functionality as Power-Down Mode 0, with the addition of the following sections:

- XTAL clock
- CEC section
- Interrupt controller section

The following pads are enabled in Power-Down Mode 1:

- Same pads as enabled in Power-Down Mode 0
- CEC pad
- INT

The internal EDID is also accessible through the DDC bus for Port A and Port B in Power-Down Mode 0 and Power-Down Mode 1.

GLOBAL PIN CONTROL

$\overline{\text{RESET}}$ Pin

The ADV7613 can be reset by a low reset pulse on the reset pin with a minimum width of 5 ms. It is recommended to wait 5 ms after the low pulse before performing an I^2C write to the ADV7613.

Reset Controls

MAIN_RESET, IO, Address 0xFF[7] (Self Clearing)

This bit controls the main reset where I^2C registers are reset to their default values.

Table 10. MAIN_RESET Function Description

MAIN_RESET	Description
0 (default)	Normal operation
1	Applies main I^2C reset

Tristate Output Drivers

PADS_PDN, IO, Address 0x0C[0]

This bit is the power-down control for pads of the digital outputs. When enabled, the pads are tristated and the input path is disabled. This control applies to INT.

Table 11. PDS_PDN Function Description

PADS_PDN	Description
0 (default)	Powers up pads of digital output pins
1	Powers down pads of digital output pins

Tristate Audio Output Drivers

TRI_AUDIO allows the user to tristate the drivers of the following audio output signals: AP0, AP1, AP2, AP3, AP4, AP5, SCLK, and MCLKOUT.

The drive strength for the output pins can be controlled by the DR_STR[1:0] bits. The ADV7613 does not support tristating via a dedicated pin.

TRI_AUDIO, IO, Address 0x15[4]

This bit is the control to tristate the audio output interface pins (AP0 to AP5).

Table 12. TRI_AUDIO Function Description

TRI_AUDIO	Description
0	Audio output pins active
1 (default)	Tristates audio output pins

Drive Strength Selection

DR_STR

It may be desirable to strengthen or weaken the drive strength of the output drivers for electromagnetic compatibility (EMC) and crosstalk reasons. This section describes the controls to adjust the output drivers used by the CP and HDMI modes.

The DR_STR[1:0] drive strength bits affect output drivers for the following output pins:

- AP0 to AP5
- SCLK
- SDA
- SCL

Digital Synthesizer Controls

The ADV7613 features two digital encoder synthesizers that generate the following clocks:

- Video DPLL: this clock synthesizer generates the pixel clock. It undoes the effect of deep color and pixel repetition that are inherent to HDMI streams. The output of the LLC pin is either this pixel clock or a divided down version, depending on the datapath configuration. It takes less than one video frame for this synthesizer to lock.
- Audio DPLL: this clock synthesizer generates the audio clock. As per HDMI specification, the incoming HDMI clock is divided down by CTS and then multiplied up by N. This audio clock is used as the main clock in the audio stream section. The output of MCLKOUT represents this clock. It takes less than 5 ms after a valid ACR packet for this synthesizer to lock.

Crystal Frequency Selection

The ADV7613 supports 28.63636 MHz frequency crystal. Following control allows selecting crystal frequency.

XTAL_FREQ_SEL[1:0], IO, Address 0x04[2:1]

These bits are the control to set the XTAL frequency used.

Table 13. XTAL_FREQ_SEL[1:0] Function Description

XTAL_FREQ_SEL[1:0]	Description
00	Reserved
01 (default)	28.63636 MHz
10	Reserved
11	Reserved

PRIMARY MODE AND VIDEO STANDARD

Setting the primary mode and choosing a video standard are the most fundamental settings when configuring the ADV7613. There are two primary modes for the ADV7613: HDMI component and HDMI graphic modes. Set the appropriate mode using PRIM_MODE[3:0].

In HDMI modes, the ADV7613 can receive and decode HDMI or DVI data throughout the DVI/HDMI receiver front end. Video data from the HDMI receiver is routed to the CP block while audio data is available on the audio interface. One of these modes is enabled by selecting either the HDMI component or the HDMI graphics primary mode.

Note that the HDMI receiver decodes and processes any applied HDMI stream irrespective of the video resolution. However, many primary mode and video standard combinations can be used to define how the decoded video data routed to the DPP and CP blocks is processed. This allows free run features and data decimation modes that some systems may require.

If free run and decimation are not required, it is recommended to set the following configuration for HDMI mode:

- PRIM_MODE[3:0] = 0x06
- VID_STD[5:0] = 0x02

PRIMARY MODE AND VIDEO STANDARD CONTROLS

PRIM_MODE[3:0], IO, Address 0x01[3:0]

A control to select the primary mode of operation of the decoder. Setting the appropriate HDMI mode is important for free run mode to work properly. This control is used with VID_STD[5:0].

Table 14. PRIM_MODE[3:0] Function Description

PRIM_MODE[3:0]	Description
0000	Reserved
0001	Reserved
0010	Reserved
0011	Reserved
0100	Reserved
0101	HDMI component
0110 (default)	HDMI graphics
0111 to 1111	Reserved

VID_STD[5:0], IO, Address 0x00[5:0]

Sets the input video standard mode. Configuration is dependent on PRIM_MODE[3:0]. Setting the appropriate mode is important for free run mode to work properly.

Table 15. VID_STD[5:0] Function Description

VID_STD[5:0]	Description
000010	Default value

Use PRIM_MODE[3:0] with VID_STD[5:0] to select the required video mode. These controls are set according to Table 16.

Table 16. Primary Mode and Video Standard Selection

PRIM_MODE[3:0]		VID_STD[5:0]				
Code	Description	Processor	Code	Input Video	Output Resolution	Comments
0101	HDMI Component (Component video)	CP	000000	Reserved	Reserved	HDMI receiver support
		CP	000001	Reserved	Reserved	
		CP	000010	Reserved	Reserved	
		CP	000011	Reserved	Reserved	
			000100	Reserved	Reserved	
			000101	Reserved	Reserved	
			000110	Reserved	Reserved	
			000111	Reserved	Reserved	
			001000	Reserved	Reserved	
			001001	Reserved	Reserved	
		CP	001010	PR 1 × 1 525p	720 × 480	

PRIM_MODE[3:0]		VID_STD[5:0]				
Code	**Description**	**Processor**	**Code**	**Input Video**	**Output Resolution**	**Comments**
		CP	001011	PR 1 × 1 625p	720 × 576	
		CP	001100	PR 2 × 1 525p	720 × 480	
		CP	001101	PR 2 × 1 625p	720 × 576	
			001110	Reserved	Reserved	
			001111	Reserved	Reserved	
			010000	Reserved	Reserved	
			010001	Reserved	Reserved	
			010010	Reserved	Reserved	
		CP	010011	HD 1 × 1	1280 × 720	
		CP	010100	HD 1 × 1	1920 × 1080	
		CP	010101	HD 1 × 1	1920 × 1035	
		CP	010110	HD 1 × 1	1920 × 1080	
			011000	Reserved	Reserved	
		CP	011001	HD 2 × 1 720p	1280 × 720	
		CP	011010	HD 2 × 1 1125	1920 × 1080	
		CP	011011	HD 2 × 1 1125	1920 × 1035	
		CP	011100	HD 2 × 1 1250	1920 × 1080	
		CP	011110	HD 1 × 1	1920 × 1080	
		CP	011111	HD 1 × 1	1920 × 1080	
0110	HDMI Graphic (Graphics)	CP	000000	SVGA	800 × 600 at 56 Hz	HDMI receiver support
		CP	000001	SVGA	800 × 600 at 60 Hz	
		CP	000010	SVGA	800 × 600 at 72 Hz	
		CP	000011	SVGA	800 × 600 at 75 Hz	
		CP	000100	SVGA	800 × 600 at 85 Hz	
		CP	000101	SXGA	1280 × 1024 at 60 Hz	
		CP	000110	SXGA	1280 × 1024 at 75 Hz	
			000111	Reserved	Reserved	
		CP	001000	VGA	640 × 480 at 60 Hz	
		CP	001001	VGA	640 × 480 at 72 Hz	
		CP	001010	VGA	640 × 480 at 75 Hz	
		CP	001011	VGA	640 × 480 at 85 Hz	
		CP	001100	XGA	1024 × 768 at 60 Hz	
		CP	001101	XGA	1024 × 768 at 70 Hz	
		CP	001110	XGA	1024 × 768 at 75 Hz	
		CP	001111	XGA	1024 × 768 at 85 Hz	
		CP	01xxxx	Reserved	Reserved	
		CP	10000	WXGA	1280 × 768 at 60 Hz	
		CP	10001	WXGA-R[1]	1280 × 768 at 60 Hz	
		CP	10010	WXGA+	1360 × 768 at 60 Hz	
		CP	10011	WXGA	1366 × 768 at 60 Hz	
		CP	10111	Reserved	Reserved	
		CP	11000	Reserved	Reserved	
		CP	11001	Reserved	Reserved	

[1] R means reduced blanking.

V_FREQ

This control is set to allow free run to work correctly (see Table 18).

V_FREQ[2:0], IO, Address 0x01[6:4]

These bits are the control to set the vertical frequency.

Table 17. V_FREQ[2:0] Function Description

V_FREQ[2:0]	Description
000 (default)	60 Hz
001	50 Hz
010	30 Hz
011	25 Hz
100	24 Hz
101	Reserved
110	Reserved
111	Reserved

HDMI DECIMATION MODES

Some of the modes defined by VID_STD have an inherent 2 × 1 decimation. For these modes, the main clock generator and the decimation filters in the DPP block are configured automatically, which ensures that the correct data rate at the input to the CP block. See the Data Preprocessor, Color Space Conversion, and Color Controls section for more information on the automatic configuration of the DPP block.

The ADV7613 correctly decodes and processes any incoming HDMI stream with the required decimation, irrespective of its video resolution.

In 1×1 mode (that is, without decimation), as long the PRIM_MODE and VID_STD registers are programmed for any HDMI mode without decimation. For example:

- Set PRIM_MODE to 0x5 and VID_STD to 0x00
- Set PRIM_MODE to 0x5 and VID_STD to 0x13
- Set PRIM_MODE to 0x6 and VID_STD to 0x02

In 2 × 1 decimation mode, as long the PRIM_MODE and VID_STD registers are programmed for any HDMI mode with 2 × 1 decimation. For example:

- Set PRIM_MODE to 0x5 and VID_STD to 0x0C
- Set PRIM_MODE to 0x5 and VID_STD to 0x19

Note that decimating the video data from an HDMI stream is optional; decimate the video data from an HDMI stream only if it is required by the downstream devices connected to the ADV7613.

PRIMARY MODE AND VIDEO STANDARD CONFIGURATION FOR HDMI FREE RUN

If free run is enabled in HDMI mode, PRIM_MODE[3:0] and VID_STD[5:0] specify the input resolution expected by the ADV7613 (for Free Run Mode 1) and/or the output resolution to which the ADV7613 free runs (for Free Run Mode 0 and Free Run Mode 1). See the Free Run Mode section for additional details on the free run feature for HDMI inputs.

RECOMMENDED SETTINGS FOR HDMI INPUTS

This section provides the recommended settings for an HDMI input encapsulating a video resolution corresponding to a selection video ID code described in the EIA/CEA-861 specification.

Table 18 provides the recommended settings for the following registers:

- PRIM_MODE
- VID_STD
- V_FREQ (do not set V_FREQ to 0x0 if not specified in Table 18)

Table 18. Recommended Settings for HDMI Inputs

Video ID Codes (861 Specification)	Formats	Pixel Repetition	Recommended Settings if Free Run Used and DIS_AUTOPRAM_BUFFER = 0	Recommended Settings if Free Run Not Used or Free Run Used and DIS_AUTO_PARAM_BUFFER = 1
2, 3	720 × 480p at 60 Hz	0	PRIM_MODE = 0x5, VID_STD = 0xA	PRIM_MODE = 0x6, VID_STD = 0x2
4	1280 × 720p at 60 Hz	0	PRIM_MODE = 0x5, VID_STD = 0x13	PRIM_MODE = 0x6, VID_STD = 0x2
14, 15	1440 × 480p at 60 Hz	1	PRIM_MODE = 0x5, VID_STD = 0xA	PRIM_MODE = 0x6, VID_STD = 0x2
16	1920 × 1080p at 60 Hz	0	PRIM_MODE = 0x5, VID_STD = 0x1E	PRIM_MODE = 0x6, VID_STD = 0x2
17, 18	720 × 576p at 60 Hz	0	PRIM_MODE = 0x5, VID_STD = 0xB	PRIM_MODE = 0x6, VID_STD = 0x2
19	1280 × 720p at 50 Hz	0	PRIM_MODE = 0x5, VID_STD = 0xA3, V_FREQ = 0x1	PRIM_MODE = 0x6, VID_STD = 0x2
29, 30	144 0× 576p at 60 Hz	1	PRIM_MODE = 0x5, VID_STD = 0xA	PRIM_MODE = 0x6, VID_STD = 0x2
31	1920 × 1080p at 50 Hz	0	PRIM_MODE = 0x5, VID_STD = 0x1E, V_FREQ = 0x1	PRIM_MODE = 0x6, VID_STD = 0x2
32	1920 × 1080p at 24 Hz	0	PRIM_MODE = 0x5, VID_STD = 0x1E, V_FREQ = 0x4	PRIM_MODE = 0x6, VID_STD = 0x2
33	1920 × 1080p at 25 Hz	0	PRIM_MODE = 0x5, VID_STD = 0x1E, V_FREQ = 0x3	PRIM_MODE = 0x6, VID_STD = 0x2
35, 36	2880 × 480p at 60 Hz	3	PRIM_MODE = 0x5, VID_STD = 0xA	PRIM_MODE = 0x6, VID_STD = 0x2
37, 38	2880 × 576p at 60 Hz	3	PRIM_MODE = 0x5, VID_STD = 0xA	PRIM_MODE = 0x6, VID_STD = 0x2
Not applicable	SVGA 800 × 600p at 56 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x0
Not applicable	SVGA 800 × 600p at 60 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x1
Not applicable	SVGA 800 × 600p at 72 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x2
Not applicable	SVGA 800 × 600p at 75 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x3
Not applicable	SVGA 800 × 600p at 85 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x04
Not applicable	SXGA 1280 × 1024p at 60 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x05
Not applicable	SXGA 1280 × 1024p at 75 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x06
Not applicable	VGA 640 × 480p at 60 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x08
Not applicable	VGA 640 × 480p at 72 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x09
Not applicable	VGA 640 × 480p at 75 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x0A
Not applicable	VGA 640 × 480p at 85 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x0B
Not applicable	VGA 1024 × 768p at 60 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x0C
Not applicable	VGA 1024 × 768p at 70 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x0D
Not applicable	VGA 1024 × 768p at 75 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x0E
Not applicable	VGA 1024 × 768p at 85 Hz	0	PRIM_MODE = 0x06, VID_STD = 0x0	PRIM_MODE = 0x06, VID_STD = 0x0F

HDMI RECEIVER

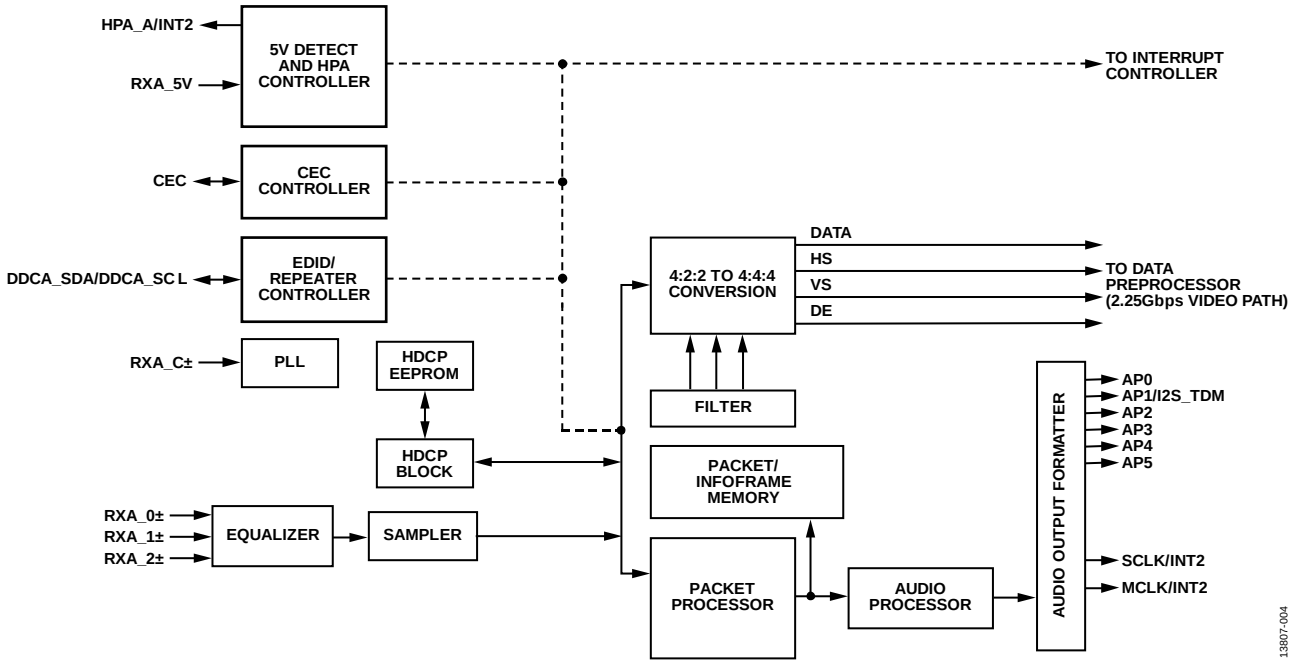


Figure 4. Functional Block Diagram of HDMI Core

The ADV7613 features an HDMI 1.4a-compliant HDMI receiver capable of supporting an HDMI stream with bit rates of up to 2.25 Gbps data bandwidth.

+5 V CABLE DETECT

The HDMI receiver in the ADV7613 can monitor the level on the +5 V power signal pin of each connected HDMI port. The results of this detection can be read back from the following I^2C registers. These readbacks are valid even when the part is not configured for HDMI mode.

CABLE_DET_A_RAW, IO, Address 0x6F[0] (Read Only)

This bit is the raw status of the Port A, +5 V cable detection signal.

Table 19. CABLE_DET_A_RAW Function Description

CABLE_DET_A_RAW	Description
0 (default)	No cable detected on Port A
1	Cable detected on Port A (high level on RXA_5V)

The ADV7613 provides a digital glitch filter on the +5 V power signals from the HDMI port. The output of this filter is used to reset the HDMI block (see the HDMI Section Reset Strategy section).

The +5 V power signal must be constantly high for the duration of the timer (controlled byFILT_5V_DET_TIMER[6:0]); otherwise, the output of the filter is low. The output of the filter returns low as soon as any change in the +5 V power signal is detected.

FILT_5V_DET_DIS, Address 68 (HDMI), Address 0x56[7]

Use this control to disable the digital glitch filter on the HDMI 5 V detect signals. The filtered signals are used as interrupt flags and used to reset the HDMI section. The filter works from an internal ring oscillator clock and, therefore, is available in power-down mode. The clock frequency of the ring oscillator is 42 MHz ± 10%.

Table 20. FILT_5V_DET_DIS Function Description

FILT_5V_DET_DIS	Description
0 (default)	Enabled
1	Disabled

Note that if the +5 V pins are not used and are left unconnected, the +5 V detect circuitry must be disconnected from the HDMI reset signal by setting DIS_CABLE_DET_RST to 1 to avoid holding the HDMI section in reset.

FILT_5V_DET_TIMER[6:0], Address 68 (HDMI), Address 0x56[6:0]

Use this control to set the timer for the digital glitch filter on the HDMI +5 V detect inputs. The unit of this parameter is two clock cycles of the ring oscillator (approximately 47 ns). The input must be constantly high for the duration of the timer; otherwise, the filter output remains low. The output of the filter returns low as soon as any change in the +5 V power signal is detected.

Table 21. FILT_5V_DET_TIMER[6:0] Function Description

FILT_5V_DET_TIMER[6:0]	Description
1011000 (default)	Approximately 4.2 µs.
xxxxxxx	Time duration of +5 V deglitch filter. The unit of this parameter is 2 clock cycles of the ring oscillator (~47 ns)

DIS_CABLE_DET_RST, Address 68 (HDMI), Address 0x48[6]

This control disables the reset effects of cable detection. DIS_CABLE_DET_RST must be set to 1 if the +5 V pins are unused and left unconnected.

Table 22. DIS_CABLE_DET_RST Function Description

DIS_CABLE_DET_RST	Description
0 (default)	Resets HDMI section if 5 V input pin corresponding to selected HDMI port (for example, RXA_5V for Port A) is inactive
1	Does not use 5 V input pins as reset signal for HDMI section

HOT PLUG ASSERT

The ADV7613 features hot plug assert (HPA) control for its HDMI port. The purpose of the control and its corresponding output pin is to communicate to an HDMI transmitter that it is possible to access the enhanced-extended display identification (E-EDID) connected to the DDC bus.

HPA_MANUAL, Address 68 (HDMI), Address 0x6C[0]

This bit is the manual control enable for the HPA output pins. Automatic control of these pins is disabled by setting this bit. Manual control is determined by the HPA_MAN_VALUE_A.

Table 23. HPA_MANUAL Function Description

HPA_MANUAL	Description
0 (default)	HPA takes its value based on HPA_AUTO_INT_EDID
1	HPA takes its value from HPA_MAN_VALUE_A

HPA_MAN_VALUE_A, IO, Address 0x20[7]

A manual control for the value of HPA on Port A. Valid only if HPA_MANUAL is set to 1.

Table 24. HPA_MAN_VALUE_A Function Description

HPA_MAN_VALUE_A	Description
0	0 V applied to HPA_A pin
1 (default)	High level applied to HPA_A pin

Note that the HPA_A pin is open drain. An external pull-up resistor is required to pull it high.

HPA_AUTO_INT_EDID[1:0], Address 68 (HDMI), Address 0x6C[2:1]

This control selects the type of automatic control on the HPA output pins. These bits have no effect when HPA_MANUAL is set to 1.

Table 25. HPA_AUTO_INT_EDID[1:0] Function Description

HPA_AUTO_INT_EDID[1:0]	Description
00	HPA of an HDMI port asserted high immediately after internal EDID activated for that port. HPA of a specific HDMI port deasserted low immediately after internal E-EDID is deactivated for that port.
01 (default)	HPA of an HDMI port asserted high following a programmable delay after part detects an HDMI cable plug on that port. HPA of an HDMI port immediately deasserted after part detects a cable disconnect on that HDMI port.

HPA_AUTO_INT_EDID[1:0]	Description
10	HPA of an HDMI port asserted high after two conditions met. 1. Internal EDID is active for that port. 2. Delayed version of cable detect signal CABLE_DET_X_RAW for that port is high. HPA of an HDMI port immediately deasserted after either of these two conditions are met: 1. Internal EDID is de-activated for that port. 2. Cable detect signal CABLE_DET_X_RAW for that port is low.
11	HPA of an HDMI port is asserted high after three conditions are met: 1. Internal EDID is active for that port. 2. Delayed version of cable detect signal CABLE_DET_X_RAW for that port is high. 3. User has set manual HPA control for that port to 1 via HPA_MAN_VALUE_X controls. HPA of an HDMI port immediately deasserted after any of these three conditions met: 1. Internal EDID de-activated for that port. 2. Cable detect signal CABLE_DET_X_RAW for that port is low. 3. User sets the manual hot plug detect (HPD) control for that port to 0 via HPA_MAN_VALUE_X controls.

Note that the delay is programmable via HPA_DELAY_SEL[3:0]. See the EDID_A_ENABLE register (Table 31) for details on enabling the internal E-EDID for an HDMI port. In HPA_MAN_VALUE_x and CABLE_DET_x_RAW, x refers to A and B.

HPA_DELAY_SEL[3:0], Address 68 (HDMI), Address 0x6C[7:4]

HPA_DELAY_SEL[3:0] sets a delay between +5 V detection and hot plug assertion on the HPA output pins, in increments of 100 ms per bit.

Table 26. HPA_DELAY_SEL[3:0] Function Description

HPA_DELAY_SEL[3:0]	Description
0000	No delay
0001	100 ms delay
0010	200 ms delay
1010 (default)	1 sec delay
1111	1.5 sec delay

HPA_TRISTATE_A, IO, Address 0x20[3]

This bit tristates the HPA output pin for Port A.

Table 27. HPA_TRISTATE_A Function Description

HPA_TRISTATE_A	Description
0 (default)	HPA_A pin active
1	Tristates HPA_A pin

HPA_STATUS_PORT_A, IO, Address 0x21[3] (Read Only)

This bit is the readback of the HPA status for Port A.

Table 28. HPA_STATUS_PORT_A Function Description

HPA_STATUS_PORT_A	Description
0 (default)	+5 V not applied to HPA_A pin by chip
1	+5 V applied to HPA_A pin by chip

HPA_OVR_TERM, Address 68 (HDMI), Address 0x6C[3]

This bit sets the termination control to be overridden by the HPA setting. When this bit is set, termination on a specific port is set according to the HPA status of that port.

Table 29. HPA_OVR_TERM Function Description

HPA_OVR_TERM	Description
0 (default)	Automatic or manual I^2C control of port termination
1	Termination controls disabled and overridden by HPA controls

E-EDID/REPEATER CONTROLLER

The HDMI section incorporates an E-EDID/repeater controller, which performs the following tasks:

- Computes the E-EDID checksum for each port
- Performs the repeater routines described in the Repeater Support section

The E-EDID/repeater controller is powered from the DVDD supply and clocked by an internal ring oscillator. The controller and the internal DDC bus arbiter are kept active in power-down Mode 0 and power-down Mode 1. This allows the internal E-EDID to be functional and accessible through the DDC port, even when the part is powered down (see the Power-Down Modes section). These HDMI transmitters can then read the capabilities of the powered-down application integrating the ADV7613 by accessing its internal E-EDID through the DDC ports.

The E-EDID/repeater controller is reset when the DVDD supplies go low or when HDCP_REPT_EDID_RESET is set high. When the E-EDID/repeater controller reboots, it performs the following tasks:

- Clears the internal E-EDID and key selection vector (KSV) RAM (see the E-EDID Data Configuration section and the Internal HDCP Key OTP ROM section)
- Updates the source physical address (SPA) registers

HDCP_REPT_EDID_RESET, Address 68 (HDMI), Address 0x5A[3] (Self Clearing)

HDCP_REPT_EDID_RESET is a reset control for the E-EDID/repeater controller. When asserted, it resets the E-EDID/repeater controller.

Table 30. HDCP_REPT_EDID_RESET Function Description

HDCP_REPT_EDID_RESET	Description
0 (default)	Normal operation
1	Resets the E-EDID/repeater controller

E-EDID DATA CONFIGURATION

The ADV7613 features a RAM that can store an E-EDID. This internal E-EDID feature can be used for both HDMI ports A and B.

The following controls are provided to enable the internal E-EDID for each of the two HDMI ports.

EDID_A_ENABLE, Address 64 (Repeater), Address 0x74[0]

This bit enables I^2C access to the internal EDID RAM from DDC Port A.

Table 31. EDID_A_ENABLE Function Description

EDID_A_ENABLE	Description
0 (default)	Disables E-EDID for Port A
1	Enables E-EDID for Port A

EDID_A_ENABLE_CPU, Address 64 (Repeater), Address 0x76[0] (Read Only)

This bit flags internal EDID enabling on Port A.

Table 32. EDID_A_ENABLE_CPU Function Description

EDID_A_ENABLE_CPU	Description
0 (default)	Disabled
1	Enabled

Note the following:

- When the internal E-EDID is enabled, the corresponding enable control (such as EDID_A_ENABLE) must be set high in a single I^2C write to ensure the fastest calculation of the checksums.
- If the internal E-EDID RAM is enabled for Port A, an external E-EDID storage device must not be connected on the DDC bus of that port.
- The internal E-EDID can be read by current address read sequences on the DDC port.
- The ADV7613 supports the segment pointer, which is set at Device Address 0x60 through the DDC bus, and used in combination with the internal E-EDID address (0xA0) to access the internal E-EDID.
- The contents of the EDID RAM are not to be trusted after power up or hardware reset. The user must write proper contents to the EDID RAM memory inside the ADV7613 via an external MCU.

E-EDID Support for Power-Down Modes

The ADV7613 supports E-EDID access in Power-Down Mode 0 and Power-Down Mode 1. Using this feature, an application that integrates the ADV7613 in standby can make its E-EDID available to the HDMI transmitter. This allows support of CEC and provides compatibility with HDMI transmitters that require the E-EDID to be available when the HDMI receiver is powered down.

In Power-Down Mode 0, the device operates in a very low power state with only the minimum of internal circuitry enabled for the internal E-EDID.

For more details on E-EDID accessibility in power-down modes, see the Power-Down Modes section.

TRANSITIONING OF POWER MODES

If the device starts in Power-Down Mode 0 and then transitions into a different power mode (that is, Power-Down Mode 1 or normal operation mode), the information in the internal E-EDID is not overwritten. The internal E-EDID remains active on the HDMI port for which the E-EDID has been accessed. This prevents disturbing E-EDID read requests from HDMI sources connected to the ADV7613 while it is being powered on, or while the power mode is transitioning.

It is possible to disable the automatic enable of internal EDID on the HDMI ports when the device comes out of power-down mode, by setting the DISABLE_AUTO_EDID bit.

DISABLE_AUTO_EDID, Address 64 (Repeater), Address 0x7A[1]

This bit disables all automatic enables for internal E-EDID.

Table 33. DISABLE_AUTO_EDID Function Description

DISABLE_AUTO_EDID	Description
0 (default)	Automatic enable of internal E-EDID on HDMI port when the part comes out of Power-Down Mode 0
1	Disable automatic enable of internal E-EDID on HDMI port when the part comes out of Power-Down Mode 0

STRUCTURE OF INTERNAL E-EDID FOR PORT A

The internal E-EDID is enabled on Port A by setting EDID_A_ENABLE to 1 (see Table 31). The structure of the internal E-EDID that is accessible on the DDC line of Port A is shown in Figure 5. The image of the internal E-EDID that is accessed on the DDC bus of Port A corresponds to the data image contained in the internal E-EDID RAM.

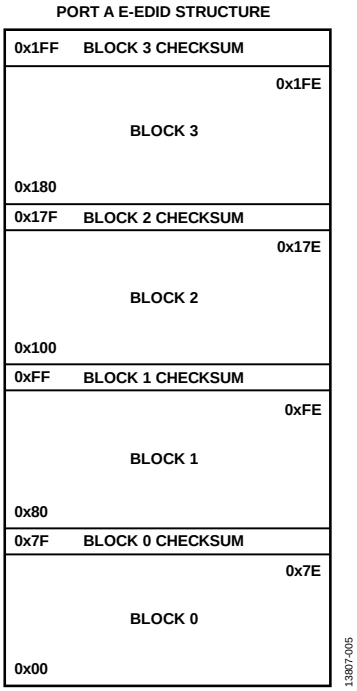


Figure 5. Port A E-EDID Structure and Mapping

Note the following:

- After EDID_A_ENABLE is set to 1, the ADV7613 E-EDID/repeater controller calculates the four checksums of the E-EDID image for Port A and updates the 0x7F, 0xFF, 0x17F, and 0x1FF internal RAM address locations in the internal E-EDID RAM with the computed checksums.
- After power up, the ADV7613 E-EDID/repeater controller sets all bytes in the internal E-EDID RAM to 0, this operation takes less than 1 ms. It is recommended to wait for at least 1 ms before initializing the EDID map with an E-EDID image.
- When internal E-EDID is enabled on Port A, the hot plug must not be asserted until the EDID map has been completely initialized with E-EDID.
- The internal E-EDID can be accessed in read-only mode through the DDC interface at the I²C Address 0xA0.
- The internal E-EDID can be accessed in read/write mode through the general I²C interface at the EDID map I²C address.

TMDS EQUALIZATION

The ADV7613 incorporates active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at long lengths and higher frequencies. The ADV7613 is capable of equalizing for cable lengths up to 30 meters and for pixel clock frequencies up to 300 MHz.

Note that transition minimized differential signaling (TMDS) equalization frequency of the active HDMI port can be read back in the TMDSFREQ[8:0] and TMDSFREQ_FRAC[6:0] registers.

PORT SELECTION

HDMI_PORT_SELECT allows the selection of the active HDMI port. This register must be set to activate HDMI Port A.

HDMI_PORT_SELECT, Address 68 (HDMI), Address 0x00 [0]

This control is used for HDMI primary port selection.

Table 34. HDMI_PORT_SELECT Function Description

HDMI_PORT_SELECT	Description
000 (default)	Port A

TMDS CLOCK ACTIVITY DETECTION

The ADV7613 provides circuitry to monitor TMDS clock activity on each of its HDMI ports. The firmware can poll the appropriate registers for TMDS clock activity detection and configure the ADV7613 as desired. TMDS clock detection control is active as soon as the ADV7613 detects activity above a 25 MHz on the TMDS clock input.

TMDS_CLK_A_RAW, IO, Address 0x6A[4] (Read Only)

TMDS_CLK_A_RAW is the raw status of the Port A TMDS clock detection signal.

Table 35. TMDS_CLK_A_RAW Function Description

TMDS_CLK_A_RAW	Description
0 (default)	No TMDS clock detected on Port A
1	TMDS clock detected on Port A

It is important to note that the clock detection flag is valid if the device is powered up or in Power Down Mode 1 (see the Power-Down Mode 1 section). The clock detection flags is valid, irrespective of the mode the part is set into via the PRIM_MODE[3:0] register.

Clock and Data Termination Control

The ADV7613 provides controls for the TMDS clock and data termination on all HDMI ports. The ADV7613 also offers automatic manual termination closure of the selected port, and individual manual control over the HDMI ports.

Note that the clock termination of the port by HDMI_PORT_SELECT must always be enabled.

The device does not support HDMI streams with clock rates lower than 25 MHz.

TERM_AUTO, Address 68 (HDMI), Address 0x01[0]

This bit allows the user to select automatic or manual control of clock termination. If automatic mode termination is enabled, then the termination on the port selected via HDMI_PORT_SELECT[1:0] is enabled. The termination is disabled on all other ports

Table 36. TERM_AUTO Function Description

TERM_AUTO	Description
0 (default)	Disable termination automatic control
1	Enable termination automatic control

Note that, to enable the fast switching feature, the termination must be set manually for each port.

When manual mode is enabled, the termination for each port is set individually by the CLOCK_TERMx_DISABLE control bits (were x is A or B).

CLOCK_TERMA_DISABLE, Address 68 (HDMI), Address 0x83[0]

This bit disables the clock termination on Port A. It can be used when TERM_AUTO is set to 0.

Table 37. CLOCK_TERMA_DISABLE Function Description

CLOCK_TERMA_DISABLE	Description
0	Enable Termination Port A
1 (default)	Disable Termination Port A

HDMI/DVI STATUS BITS

HDMI/DVI status mode is available through HDMI_MODE for active port and BG_HDMI_MODE for background port.

HDMI_MODE, Address 68 (HDMI), Address 0x05[7] (Read Only)

This bit is a readback to indicate whether the stream processed by the HDMI core is a DVI or an HDMI stream.

Table 38. HDMI_MODE Function Description

HDMI_MODE	Description
0 (default)	DVI mode detected
1	HDMI mode detected

BG_HDMI_MODE, Address 68 (HDMI), Address 0xEB[0] (Read Only)

This bit is a readback to indicate whether the stream processed by the HDMI core is a DVI or an HDMI stream.

Table 39. BG_HDMI_MODE Function Description

BG_HDMI_MODE	Description
0 (default)	DVI mode detected
1	HDMI mode detected

VIDEO 3D DETECTION

The status of 3D video is available through the VIDEO_3D_RAW bit.

VIDEO_3D_RAW, IO, Address 0x6A[2] (Read Only)

This bit is the raw status of the video 3D signal.

Table 40. VIDEO_3D_RAW Function Description

VIDEO_3D_RAW	Description
0	Video 3D not detected
1	Video 3D detected

TMDS MEASUREMENT

The ADV7613 contains logic that measures the frequency of the TMDS clock transmitted. The TMDS frequency can be read back via the TMDSFREQ[8:0] and TMDSFREQ_FRAC[6:0] registers.

TMDS Measurement After TMDS PLL

The TMDSFREQ measurement is provided by a clock measurement circuit located after the TMDS PLL. Therefore, TMDS PLL must be locked to the incoming TMDS clock for the TMDSFREQ and TMDSFREQ_FRAC registers to return a valid measurement. The TMDS frequency can be obtained using Equation 1, TMDS frequency in MHz (measured after TMDS PLL).

$$f_{TMDS} = TMDSFREQ + \frac{TMDSFREQ\_FRAC}{128} \quad (1)$$

The TMDS PLL lock status can be monitored via TMDS_PLL_LOCKED. Figure 6 shows the algorithm that can be implemented on an external controller to monitor the TMDS clock frequency.

The TMDS_PLL_LOCKED flag is considered valid if a TMDS clock is input on the HDMI port selected via HDMI_PORT_SELECT.

The NEW_TMDS_FRQ_RAW flag can be used to monitor if the TMDS frequency on the selected HDMI port changes by a programmable threshold.

The ADV7613 can be configured to trigger an interrupt when the NEW_TMDS_FRQ_RAW bit changes from 0 to 1. In that configuration, the NEW_TMDS_FRQ_ST interrupt status indicates that NEW_TMDS_FRQ_RAW has changed from 0 to 1. See the Interrupts section for additional information on the configuration of interrupts.

TMDSFREQ[8:0], Address 68 (HDMI), Address 0x51[7:0]; Address 0x52[7] (Read Only)

This register provides a full precision integer TMDS frequency measurement.

Table 41. TMDSFREQ[8:0] Function Description

TMDSFREQ[8:0]	Description
000000000 (default)	Outputs 9-bit TMDS frequency measurement in MHz
xxxxxxxxx	Outputs 9-bit TMDS frequency measurement in MHz

TMDSFREQ_FRAC[6:0], Address 68 (HDMI), Address 0x52[6:0] (Read Only)

This register is a readback to indicate the fractional bits of measured frequency of PLL recovered TMDS clock. The unit is 1/128 MHz.

Table 42. TMDSFREQ_FRAC[6:0] Function Description

TMDSFREQ_FRAC[6:0]	Description
0000000 (default)	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz
xxxxxxx	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz

BG_TMDSFREQ[8:0], Address 68 (HDMI), Address 0xE0[7:0]; Address 0xE1[7] (Read Only)

This register provides a precision integer TMDS frequency measurement on the background port selected by BG_MEAS_PORT_SEL[2:0]. The value provided is the result of a single measurement of the TMDS PLL frequency in MHz. This value is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1.

Table 43. BG_TMDSFREQ[8:0] Function Description

BG_TMDSFREQ[8:0]	Description
xxxxxxxxx	Outputs 9-bit TMDS frequency measurement in MHz

BG_TMDSFREQ_FRAC[6:0], Address 68 (HDMI), Address 0xE1[6:0] (Read Only)

This register provides a precision fractional measurement of the TMDS frequency on the background port selected by BG_MEAS_PORT_SEL[2:0]. The unit is 1/128 MHz and the value is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1.

Table 44. BG_TMDSFREQ_FRAC[6:0] Function Description

BG_TMDSFREQ_FRAC[6:0]	Description
xxxxxxx	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz

TMDS_PLL_LOCKED, Address 68 (HDMI), Address 0x04[1] (Read Only)

This bit is a readback to indicate if the TMDS PLL is locked to the TMDS clock input to the selected HDMI port.

Table 45. TMDS_PLL_LOCKED Function Description

TMDS_PLL_LOCKED	Description
0 (default)	The TMDS PLL is not locked.
1	The TMDS PLL is locked to the TMDS clock input to the selected HDMI port.

TMDSPLL_LCK_A_RAW, IO, Address 0x6A[6] (Read Only)

This bit is a readback to indicate the raw status of the Port A TMDS PLL lock signal.

Table 46. TMDSPLL_LCK_A_RAW Function Description

TMDSPLL_LCK_A_RAW	Description
0 (default)	TMDS PLL on Port A is not locked.
1	TMDS PLL on Port A is locked to the incoming clock.

NEW_TMDS_FRQ_RAW, IO, Address 0x83[1] (Read Only)

Status of new TMDS frequency interrupt signal. When set to 1, it indicates that the TMDS frequency has changed by more than the tolerance set in FREQTOLERANCE[3:0]. Once set, this bit remains high until it is cleared via NEW_TMDS_FREQ_CLR.

Table 47. NEW_TMDS_FRQ_RAW Function Description

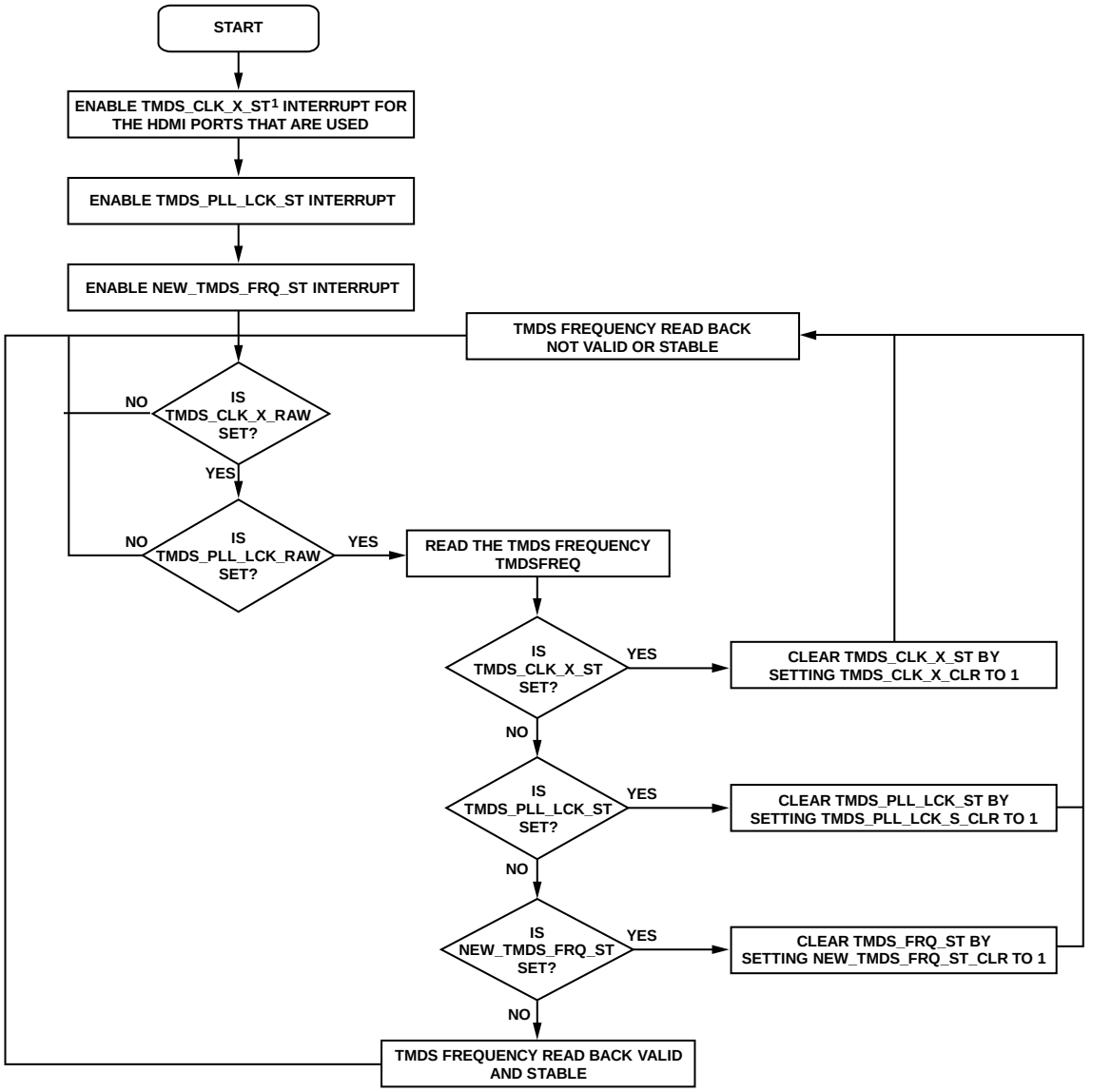
NEW_TMDS_FRQ_RAW	Description
0 (default)	TMDS frequency has not changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI map.
1	TMDS frequency has changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI map.

FREQTOLERANCE[3:0], Address 68 (HDMI), Address 0x0D[3:0]

FREQTOLERANCE[3:0] sets the tolerance in MHz for new TMDS frequency detection. This tolerance is used for the audio mute mask MT_MSK_VCLK_CHNG and the HDMI status bit NEW_TMDS_FRQ_RAW.

Table 48. FREQTOLERANCE[3:0] Function Description

FREQTOLERANCE[3:0]	Description
0100 (default)	Default tolerance in MHz for new TMDS frequency detection
xxxx	Tolerance in MHz for new TMDS frequency detection



[1]THE TMDS_CLK_X_ST INTERRUPTS FOLLOW:
TMDS_CLK_A_ST (IO MAP, REGISTER 0x6B BIT 3)
TMDS_CLK_B_ST (IO MAP, REGISTER 0x6B BIT 2)
TMDS_CLK_C_ST (IO MAP, REGISTER 0x6B BIT 1)
TMDS_CLK_D_ST (IO MAP, REGISTER 0x6B BIT 0)

Figure 6. Monitoring TMDS Clock Frequency

VIDEO FIFO

The ADV7613 contains a first in, first out (FIFO) located between the incoming TMDS data and the CP core (see Figure 7). Data arriving over the HDMI link is at 1× for non-deep color mode (8 bits per channel).

The video FIFO also provides extreme robustness to jitter on the TMDS clock. The CP clock is generated by a DPLL running on the incoming TMDS clock, and the CP clock may contain less jitter than the incoming TMDS clock. The video FIFO provides immunity to the incoming jitter and the resultant clock phase mismatch between the CP clock and the TMDS clock.

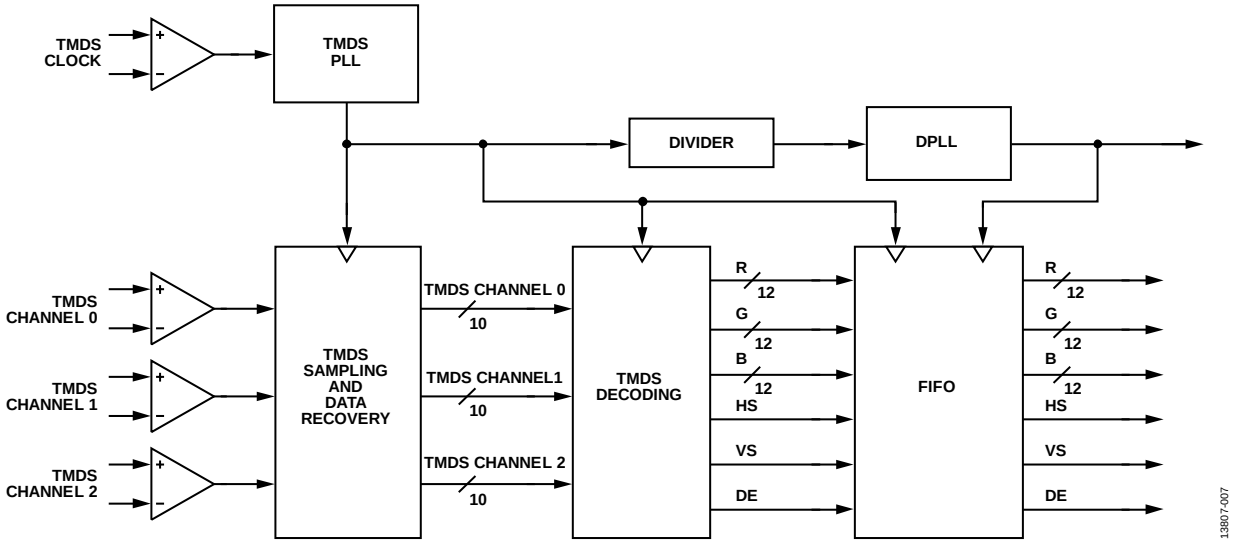


Figure 7. HDMI Video FIFO

The video FIFO operates completely autonomously. It automatically resynchronizes the read and write pointers if they are about to point to the same location. However, it is also possible for the user to observe and control the FIFO operation with a number of FIFO status and control registers.

DCFIFO_LEVEL[2:0], Address 68 (HDMI), Address 0x1C[2:0] (Read Only)

DCFIFO_LEVEL[2:0] is a readback that indicates the distance between the read and write pointers. Overflow/underflow is read as Level 0. Ideal centered functionality is read as 0b100.

Table 49. DCFIFO_LEVEL[2:0] Function Description

DCFIFO_LEVEL[2:0]	Description
000 (default)	FIFO has underflowed or overflowed.
001	FIFO is about to overflow.
010	FIFO has some margin.
011	FIFO has some margin.
100	FIFO perfectly balanced
101	FIFO has some margin.
110	FIFO has some margin.
111	FIFO is about to underflow.

DCFIFO_LOCKED, Address 68 (HDMI), Address 0x1C[3] (Read Only)

A readback to indicate if video FIFO is locked.

Table 50. DCFIFO_LOCKED Function Description

DCFIFO_LOCKED	Description
0 (default)	Video FIFO is not locked. Video FIFO had to resynchronize between previous two vertical synchronizations (VSYNCs).
1	Video FIFO is locked. Video FIFO did not have to resynchronize between previous two VSYNCs.

DCFIFO_RECENTER, Address 68 (HDMI), Address 0x5A[2] (Self Clearing)

This bit is a reset to recenter the video FIFO. This is a self clearing bit.

Table 51. DCFIFO_RECENTER Function Description

DCFIFO_RECENTER	Description
0 (default)	Video FIFO normal operation
1	Video FIFO to recenter

DCFIFO_KILL_DIS, Address 68 (HDMI), Address 0x1B[2]

The video FIFO output is zeroed if there is more than one resynchronization of the pointers within two FIFO cycles. This behavior can be disabled with this bit.

Table 52. DCFIFO_KILL_DIS Function Description

DCFIFO_KILL_DIS	Description
0 (default)	FIFO output set to zero if more than one resynchronization is necessary during two FIFO cycles
1	FIFO output never set to zero regardless of how many resynchronizations occur

DCFIFO_KILL_NOT_LOCKED, Address 68 (HDMI), Address 0x1B[3]

DCFIFO_KILL_NOT_LOCKED controls whether or not the output of the Video FIFO is set to zero when the video PLL is unlocked.

Table 53. DCFIFO_KILL_NOT_LOCKED Function Description

DCFIFO_KILL_NOT_LOCKED	Description
0	FIFO data is output regardless of video PLL lock status.
1 (default)	FIFO output is zeroed if video PLL is unlocked.

The DCFIFO is programmed to reset itself automatically when the video PLL transitions from unlocked to locked. Note that the video PLL transition does not necessarily indicate that the overall system is stable.

DCFIFO_RESET_ON_LOCK, Address 68 (HDMI), Address 0x1B[4]

DCFIFO_RESET_ON_LOCK enables the reset/recentering of video FIFO on video PLL unlock.

Table 54. DCFIFO_RESET_ON_LOCK Function Description

DCFIFO_RESET_ON_LOCK	Description
0	Do not reset on video PLL lock.
1 (default)	Reset FIFO on video PLL lock.

PIXEL REPETITION

In HDMI mode, video formats with TMDS rates below 25 M pixels/sec require pixel repetition to be transmitted over the TMDS link. When the ADV7613 receives this type of video format, it discards repeated pixel data automatically, based on the pixel repetition field available in the auxiliary video information (AVI) InfoFrame.

When HDMI_PIXEL_REPETITION is nonzero, video pixel data is discarded and the pixel clock frequency is divided by (HDMI_PIXEL_REPETITION) + 1.

HDMI_PIXEL_REPETITION[3:0], Address 68 (HDMI), Address 0x05[3:0] (Read Only)

HDMI_PIXEL_REPETITION[3:0] is a readback to provide the current HDMI pixel repetition value decoded from the AVI InfoFrame received. The HDMI receiver automatically discards repeated pixel data and divides the pixel clock frequency appropriately as per the pixel repetition value.

Table 55. HDMI_PIXEL_REPETITION[3:0] Function Description

HDMI_PIXEL_REPETITION[3:0]	Description
0000 (default)	1×
0001	2×
0010	3×
0011	4×
0100	5×
0101	6×
0110	7×
0111	8×
1000	9×
1001	10×
1010 to 1111	Reserved

DEREP_N_OVERRIDE, Address 68 (HDMI), Address 0x41[4]

This control allows the user to override the pixel repetition factor. The ADV7613 then uses DEREP_N instead of HDMI_PIXEL_REPETITION[3:0] to discard video pixel data from the incoming HDMI stream.

Table 56. DEREP_N_OVERRIDE Function Description

Function

DEREP_N_OVERRIDE	Description
0 (default)	Automatic detection and processing of procession of pixel repeated modes using the AVI InfoFrame information.
1	Enables manual setting of the pixel repetition factor as per DEREP_N[3:0].

DEREP_N[3:0], Address 68 (HDMI), Address 0x41[3:0]

DEREP_N[3:0] sets the derepetition value if derepetition is overridden by setting DEREP_N_OVERRIDE.

Table 57. DEREP_N[3:0] Function Description

Function

DEREP_N[3:0]	Description
0000 (default)	DEREP_N+1 indicates the pixel and clock discard factor

BG_PIX_REP[3:0], Address 68 (HDMI), Address 0xEA[7:4] (Read Only)

BG_PIX_REP[3:0] is the background port pixel repetition status for the background HDMI port determined by BG_MEAS_PORT_SEL[2:0]. The readback provides the pixel repetition value in AVI InfoFrame and is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1.

Table 58. BG_PIX_REP[3:0] Function Description

BG_PIX_REP[3:0]	Description
0000	1x
0001	2x
0010	3x
0011	4x
0100	5x
0101	6x
0110	7x
0111	8x
1000	9x
1001	10x
1010 to 1111	Reserved

Following registers allow forcing YCrCb 444 and YCrCb 422 regardless of the AVI InfoFrame. This feature is useful when source switches between YCrCb 444 and YCrCb 422 modes without sending appropriate update in AVI InfoFrame.

FORCE_YCRCB_444, Address 68 (HDMI), Address 0x46[4]

FORCE_YCRCB_444 forces a 4:4:4 interpretation of the video contents, regardless of the description in the AVI InfoFrame. This bit carries higher priority than FORCE_YCRCB_422.

Table 59. FORCE_YCRCB_444 Function Description

FORCE_YCRCB_444	Description
0 (default)	Not forced
1	Forced

FORCE_YCRCB_422, Address 68 (HDMI), Address 0x47[4]

FORCE_YCRCB_422 forces a 4:2:2 interpretation of the video contents, regardless of the description in the AVI InfoFrame. This bit is only valid if FORCE_YCRCB_444 is zero.

Table 60. FORCE_YCRCB_422 Function Description

FORCE_YCRCB_422	Description
0 (default)	Not forced
1	Forced

HDCP SUPPORT

HDCP Decryption Engine

The HDCP decryption engine allows the reception and decryption of HDCP content-protected video and audio data. In the HDCP authentication protocol, the transmitter authenticates the receiver by accessing the HDCP registers of the ADV7613 over the DDC bus. Once the authentication is initiated, the HDCP decryption integrated in the ADV7613 computes and updates a decryption mask for every video frame. This mask is applied to the incoming data at every clock cycle to yield decrypted video and audio data.

HDCP_A0, Address 68 (HDMI), Address 0x00[7]

HDCP_A0 is a control to set the second LSB of the HDCP port I^2C address.

Table 61. HDCP_A0 Function Description

HDCP_A0	Description
0 (default)	I^2C address for HDCP port is 0x74. Used for single-link mode or first receiver in dual-link mode.
1	I^2C address for HDCP port is 0x76. Used only for a second receiver in dual-link mode.

HDMI_CONTENT_ENCRYPTED, Address 68 (HDMI), Address 0x05[6] (Read Only)

This bit is a readback to indicate the use of HDCP encryption.

Table 62. HDMI_CONTENT_ENCRYPTED Function Description

HDMI_CONTENT_ENCRYPTED	Description
0 (default)	The input stream processed by the HDMI core is not HDCP encrypted.
1	The input stream processed by the HDMI core is HDCP encrypted.

HDMI_ENCRPT_x_RAW reports the encryption status of the data present on each individual HDMI port (where x is A or B).

Note that these bits are reset to 0 if an HDMI packet detection reset occurs (see the HDMI Packet Detection Flag Reset section).

HDMI_ENCRPT_A_RAW, IO, Address 0x6F[2] (Read Only)

This bit is the raw status of Port A encryption detection signal.

Table 63. HDMI_ENCRPT_A_RAW Function Description

HDMI_ENCRPT_A_RAW	Description
0 (default)	Current frame in Port A is not encrypted.
1	Current frame in Port A is encrypted.

The ADV7613 supports the 1.1_FEATURES, FAST_REAUTHENTICATION, and FAST_I2C speed HDCP features. The BCAPS register must be initialized appropriately if these features are to be supported by the application integrating the ADV7613. For example, set BCAPS[0] to 1 to support FAST_REAUTHENTICATION.

It is recommended to set BCAPS[7:0], Bit 7 to 1 if the ADV7613 is used as the front end of an HDMI receiver. This bit must be set to 0 for DVI applications.

Internal HDCP Key OTP ROM

The ADV7613 features an on-chip nonvolatile memory that is preprogrammed with a set of HDCP keys.

HDCP Keys Access Flags

The ADV7613 accesses the internal HDCP key, one-time programmable (OTP) ROM (also referred to as HDCP ROM) on two different occasions:

- After a power up, the ADV7613 reads the KSV from the internal HDCP ROM (see Figure 8).
- After a KSV update from an HDCP transmitter, the ADV7613 reads the KSV and all keys to carry out the link verification response (see Figure 9).

The host processor can read the HDCP_KEYS_READ and HDCP_KEY_ERROR flags to check that the ADV7613 has accessed the HDCP ROM.

HDCP_KEYS_READ, Address 68 (HDMI), Address 0x04[5] (Read Only)

HDCP_KEYS_READ is a readback to indicate a successful read of the HDCP keys and/or KSV from the internal HDCP Key OTP ROM. A logic high is returned when the read is successful.

Table 64. HDCP_KEYS_READ Function Description

HDCP_KEYS_READ	Description
0 (default)	HDCP keys and/or KSV not yet read
1	HDCP keys and/or KSV HDCP keys read

HDCP_KEY_ERROR, Address 68 (HDMI), Address 0x04[4] (Read Only)

HDCP_KEY_ERROR is a readback to indicate if a checksum error occurred while reading the HDCP and/or KSV from the HDCP key ROM Returns 1 when HDCP Key master encounters an error while reading the HDCP key OTP ROM.

Table 65. HDCP_KEY_ERROR Function Description

HDCP_KEY_ERROR	Description
0 (default)	No error occurred while reading HDCP keys
1	HDCP keys read error

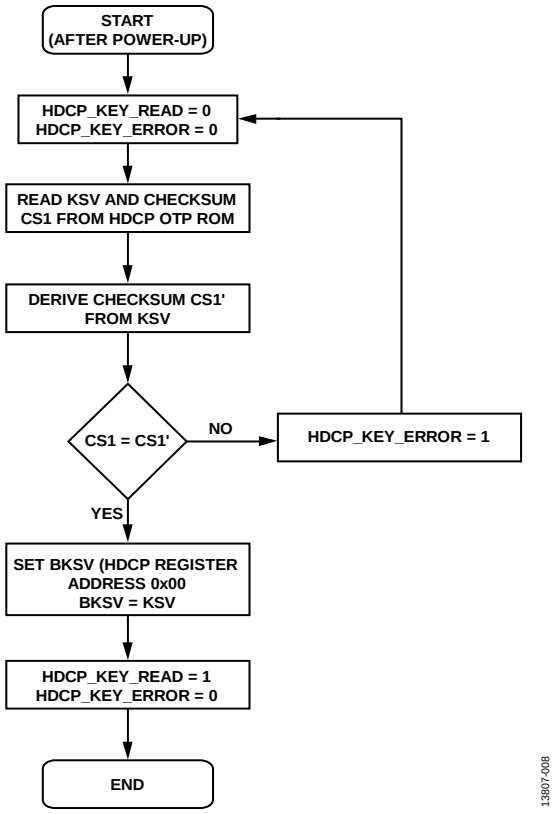


Figure 8. HDCP ROM Access After Power-Up

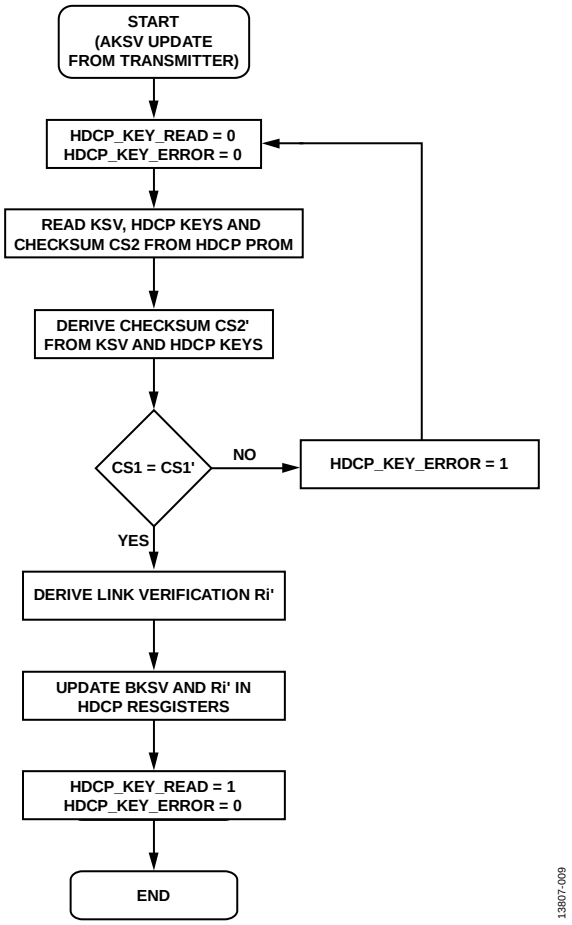


Figure 9. HDCP ROM Access After KSV Update from the Transmitter

After the device has powered up, it is recommended to wait for 1 ms before checking the HDCP_KEYS_READ and HDCP_KEY_ERROR flag bits. This ensures that the ADV7613 had sufficient time to access the internal HDCP ROM and set the HDCP_KEYS_READ and HDCP_KEY_ERROR flag bits.

After an HDCP transmitter key selection vector (AKSV) update from the transmitter, it is recommended to wait for 2 ms before checking the HDCP_KEYS_READ and HDCP_KEY_ERROR flag bits. This ensures that the ADV7613 had sufficient time to access the internal HDCP ROM, and set the HDCP_KEYS_READ and HDCP_KEY_ERROR flag bits.

When the ADV7613 successfully retrieves the HDCP keys and/or KSV from the internal HDCP ROM, the HDCP_KEYS_READ flag bit is set to 1 and the HDCP_KEY_ERROR flag bit is set to 0.

The I^2C controllers for the main I^2C lines and the HDCP lines are independent of each other. It is, therefore, possible to access the internal registers of the ADV7613 while it reads the HDCP keys and/or the KSV from the internal HDCP ROM.

A hardware reset (that is, reset via the reset pin) does not lead the ADV7613 to read the KSV or the keys from the HDCP ROM.

The ADV7613 takes 1.8 ms to read the keys from the HDCP ROM.

HDCP Ri Expired

The following register allows early detection of HDMI transmitter (Tx) failure. See also the interrupt status control, RI_EXPIRED_A_ST.

HDCP_RI_EXPIRED, Address 68 (HDMI), Address 0x04[3] (Read Only)

This bit reads back high when a calculated Ri has not been read by the source Tx on the active port. It remains high until the next AKSV update.

Table 66. HDCP_RI_EXPIRED Function Description

HDCP_RI_EXPIRED	Description
0 (default)	Calculated Ri has been read by the source Tx
1	Calculated Ri has not been read by the source Tx

HDMI SYNCHRONIZATION PARAMETERS

The ADV7613 contains the logic required to measure the details of the incoming video resolution. The HDMI synchronization parameters readback registers from the HDMI map can be used, in addition to the STDI registers from the CP (see the Standard Detection and Identification section), to estimate the video resolution of the incoming HDMI stream.

Note that the synchronization parameters are valid if the part is configured in HDMI mode via PRIM_MODE[3:0]. Also note that the HDMI synchronization filter readback parameters are valid even while the part free runs (see the Free Run Mode section) on the condition that the measurement filters have locked.

Horizontal Filter and Measurements

The HDMI horizontal filter performs measurements on the data enable (DE) and horizontal synchronization (HSYNC) of the HDMI stream on the selected port. The ADV7613 also performs horizontal measurements on the background port as selected by BG_MEAS_PORT_SEL[2:0]. These measurements are available in the HDMI map and can be used to determine the resolution of the incoming video data streams.

Primary Port Horizontal Filter Measurements

The HDMI horizontal filter performs the measurements described in this section on the HDMI port selected by HDMI_PORT_SELECT.

The horizontal measurements are valid only if DE_REGEN_LCK_RAW is set to 1.

The HDMI horizontal filter is used solely to measure the horizontal synchronization signals decoded from the HDMI stream. The HDMI horizontal filter is not in the main path of the synchronization processed by the part and does not delay the overall HDMI data into video data out latency.

The unit for horizontal filter measurement is a pixel, that is, the actual element of the picture content encapsulated in the HDMI/DVI stream, which the ADV7613 processes. A pixel has a duration T_{PIXEL}, which is provided in Equation 2, unit time of horizontal filter measurements.

$$T_{PIXEL} = T_{FTMDS} \times DEEP\_COLOR\_RATIO \times (PIXEL\_REPETITION + 1) \quad (2)$$

where:
T_{FTMDS} is the TMDS frequency.
DEEP_COLOR_RATIO = 1 for 24-bit deep color.
PIXEL_REPETITION is the number of repeated pixels in the input HDMI stream.

DE_REGEN_FILTER_LOCKED, Address 68 (HDMI), Address 0x07[5] (Read Only)

This bit shows the DE regeneration filter lock status. It indicates that the DE regeneration section has locked to the received DE and horizontal synchronization parameter measurements are valid for readback.

Table 67. DE_REGEN_FILTER_LOCKED Function Description

DE_REGEN_FILTER_LOCKED	Description
0 (default)	DE regeneration not locked
1	DE regeneration locked to incoming DE

DE_REGEN_LCK_RAW, IO, Address 0x6A[0] (Read Only)

This bit is the raw status of the DE regeneration lock signal.

Table 68. DE_REGEN_LCK_RAW Function Description

DE_REGEN_LCK_RAW	Description
0 (default)	DE regeneration block has not been locked.
1	DE regeneration block has been locked to the incoming DE signal.

TOTAL_LINE_WIDTH[13:0], Address 68 (HDMI), Address 0x1E[5:0]; Address 0x1F[7:0] (Read Only)

TOTAL_LINE_WIDTH[13:0] is the total line width is a horizontal synchronization measurement. This gives the total number of pixels per line. This measurement is valid only when the DE regeneration filter has locked.

Table 69. TOTAL_LINE_WIDTH[13:0] Function Description

TOTAL_LINE_WIDTH[13:0]	Description
xxxxxxxxxxxx	Total number of pixels per line

LINE_WIDTH[12:0], Address 68 (HDMI), Address 0x07[4:0]; Address 0x08[7:0] (Read Only)

Line width is a horizontal synchronization measurement, which gives the number of active pixels in a line. This measurement is only valid when the DE regeneration filter is locked.

Table 70. LINE_WIDTH[12:0] Function Description

LINE_WIDTH[12:0]	Description
00000000000 (default)	Total number of active pixels per line
xxxxxxxxxxx	Total number of active pixels per line

HSYNC_FRONT_PORCH[12:0], Address 68 (HDMI), Address 0x20[4:0]; Address 0x21[7:0] (Read Only)

HSYNC front porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked.

Table 71. HSYNC_FRONT_PORCH[12:0] Function Description

HSYNC_FRONT_PORCH[12:0]	Description
xxxxxxxxxxx	Total number of pixels in the front porch

HSYNC_PULSE_WIDTH[12:0], Address 68 (HDMI), Address 0x22[4:0]; Address 0x23[7:0] (Read Only)

HSYNC pulse width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked.

Table 72. HSYNC_PULSE_WIDTH[12:0] Function Description

HSYNC_PULSE_WIDTH[12:0]	Description
xxxxxxxxxxx	Total number of pixels in the HSYNC pulse

HSYNC_BACK_PORCH[12:0], Address 68 (HDMI), Address 0x24[4:0]; Address 0x25[7:0] (Read Only)

HSYNC back porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked.

Table 73. HSYNC_BACK_PORCH[12:0] Function Description

HSYNC_BACK_PORCH[12:0]	Description
xxxxxxxxxxx	Total number of pixels in the back porch

DVI_HSYNC_POLARITY, Address 68 (HDMI), Address 0x05[5] (Read Only)

This bit is a readback to indicate the polarity of the HSYNC encoded in the input stream.

Table 74. DVI_HSYNC_POLARITY Function Description

DVI_HSYNC_POLARITY	Description
0 (default)	The HSYNC is active low.
1	The HSYNC is active high.

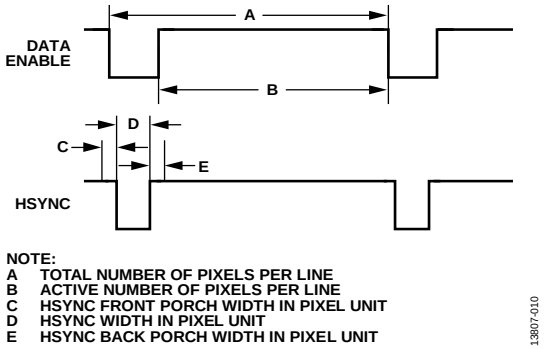


Figure 10. Horizontal Timing Parameters

Background Port Horizontal Filter Measurements

The HDMI horizontal filter performs the measurements described in this section on the HDMI port selected by BG_MEAS_PORT_SEL[2:0].

Note that BG_PARAM_LOCK must be high for background horizontal and vertical measurements to be valid.

BG_PARAM_LOCK, Address 68 (HDMI), Address 0xEA[1] (Read Only)

This bit is a flag to indicate that vertical and horizontal parameters have been locked during a background measurement.

Table 75. BG_PARAM_LOCK Function Description

BG_PARAM_LOCK	Description
0 (default)	Horizontal and vertical were not locked when measurement for select background HDMI port were taken.
1	Horizontal and vertical were locked when measurement for select background HDMI port were taken.

BG_TOTAL_LINE_WIDTH[13:0], Address 68 (HDMI), Address 0xE4[5:0]; Address 0xE5[7:0] (Read Only)

Background port total line width, a horizontal synchronization measurement for the background HDMI Port determined by BG_MEAS_PORT_SEL[2:0]. The value represents the total number of pixels in a line and is updated when a update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1.

Table 76. BG_TOTAL_LINE_WIDTH[13:0] Function Description

BG_TOTAL_LINE_WIDTH[13:0]	Description
xxxxxxxxxxxxx	The total number of pixels per line on the background measurement port

BG_LINE_WIDTH[12:0], Address 68 (HDMI), Address 0xE2[4:0]; Address 0xE3[7:0] (Read Only)

Background port line width, a horizontal synchronization measurement for the background HDMI Port determined by BG_MEAS_PORT_SEL[2:0]. The value represents the number of active pixels in a line and is updated when a update request is made via the BG_MEAS_REQ control bit.

Table 77. BG_LINE_WIDTH[12:0] Function Description

BG_LINE_WIDTH[12:0]	Description
0000000000000 (default)	The number of active pixels per line on the background measurement port.
xxxxxxxxxxxxx	The number of active pixels per line on the background measurement port.

Horizontal Filter Locking Mechanism

The locking/unlocking mechanism of the HDMI horizontal filter is as follows.

The HDMI horizontal filter locks if the following two conditions are met:

- The DE transitions occur at the exact same pixel count for eight consecutive video lines.
- The HSYNC transitions occur at the exact same pixel count for eight consecutive video lines.

The HDMI horizontal filter unlocks if either of the two following conditions are met:

- The DE transitions occur on different pixels count for 15 consecutive video lines.
- The HSYNC transitions occur on different pixels count for 15 consecutive video lines.

Vertical Filters and Measurements

The ADV7613 integrates an HDMI vertical filter that performs measurements on the vertical synchronization (VSYNC) of the HDMI stream on the selected port. The ADV7613 also performs vertical measurements on the background port as selected by BG_MEAS_PORT_SEL[2:0].These measurements are available in the HDMI map and can be used to determine the resolution of the incoming video data streams.

Primary Port Vertical Filter Measurements

The HDMI vertical filter performs the measurements on the HDMI port selected by HDMI_PORT_SELECT.

The Field 0 measurements are adequate to determine the standard of incoming progressive modes. Use a combination of Field 0 and Field 1 measurements to determine the standard of interlaced modes.

Note that the vertical measurements are valid only if V_LOCKED_RAW is set to 1. The HDMI vertical filter is used solely to measure the vertical synchronization signals decoded from the HDMI stream. This filter is not in the main path of the synchronization processed by the part and does not delay the overall HDMI data into video data out latency.

VERT_FILTER_LOCKED, Address 68 (HDMI), Address 0x07[7] (Read Only)

VERT_FILTER_LOCKED is the vertical filter lock status. Indicates whether the vertical filter is locked and vertical synchronization parameter measurements are valid for readback.

Table 78. VERT_FILTER_LOCKED Function Description

VERT_FILTER_LOCKED	Description
0	Vertical filter has not locked.
1	Vertical filter has locked.

V_LOCKED_RAW, IO, Address 0x6A[1] (Read Only)

V_LOCKED_RAW is the raw status of the vertical sync filter locked signal.

Table 79. V_LOCKED_RAW Function Description

V_LOCKED_RAW	Description
0	Vertical sync filter has not locked and vertical sync parameters are not valid
1	Vertical sync filter has locked and vertical sync parameters are valid

Note that Field 0 measurements are used to determine the video modes that are progressive.

FIELD0_TOTAL_HEIGHT[13:0], Address 68 (HDMI), Address 0x26[5:0]; Address 0x27[7:0] (Read Only)

Field 0 total height is a vertical synchronization measurement. This readback gives the total number of half lines in Field 0. This measurement is valid only when the vertical filter has locked.

Table 80. FIELD0_TOTAL_HEIGHT[13:0] Function Description

FIELD0_TOTAL_HEIGHT[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in Field 0 (divide readback by 2 to get number of lines)

FIELD0_HEIGHT[12:0], Address 68 (HDMI), Address 0x09[4:0]; Address 0x0A[7:0] (Read Only)

Field 0 height is a vertical filter measurement. This readback gives the number of active lines in Field 0. This measurement is valid only when the vertical filter has locked.

Table 81. FIELD0_HEIGHT[12:0] Function Description

FIELD0_HEIGHT[12:0]	Description
xxxxxxxxxxxxx	The number of active lines in Field 0

FIELD0_VS_FRONT_PORCH[13:0], Address 68 (HDMI), Address 0x2A[5:0]; Address 0x2B[7:0] (Read Only)

Field 0 VSYNC front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. This measurement is valid only when the vertical filter has locked.

Table 82. FIELD0_VS_FRONT_PORCH[13:0] Function Description

FIELD0_VS_FRONT_PORCH[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in the VSYNC front porch of Field 0 (divide readback by 2 to get number of lines)

FIELD0_VS_PULSE_WIDTH[13:0], Address 68 (HDMI), Address 0x2E[5:0]; Address 0x2F[7:0] (Read Only)

Field 0 VSYNC width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked.

Table 83. FIELD0_VS_PULSE_WIDTH[13:0] Function Description

FIELD0_VS_PULSE_WIDTH[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in the VSYNC pulse of Field 0 (divide readback by 2 to get number of lines)

FIELD0_VS_BACK_PORCH[13:0], Address 68 (HDMI), Address 0x32[5:0]; Address 0x33[7:0] (Read Only)

Field 0 VSYNC back porch width is a vertical synchronization measurement. The unit for this measurement is half lines.

Table 84. FIELD0_VS_BACK_PORCH[13:0] Function Description

FIELD0_VS_BACK_PORCH[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in the VSYNC back porch of Field 0 (divide readback by 2 to get number of lines)

DVI_VSYNC_POLARITY, Address 68 (HDMI), Address 0x05[4] (Read Only)

DVI_VSYNC_POLARITY is a readback to indicate the polarity of the VSYNC encoded in the input stream.

Table 85. DVI_VSYNC_POLARITY Function Description

DVI_VSYNC_POLARITY	Description
0	The VSYNC is active low.
1	The VSYNC is active high.

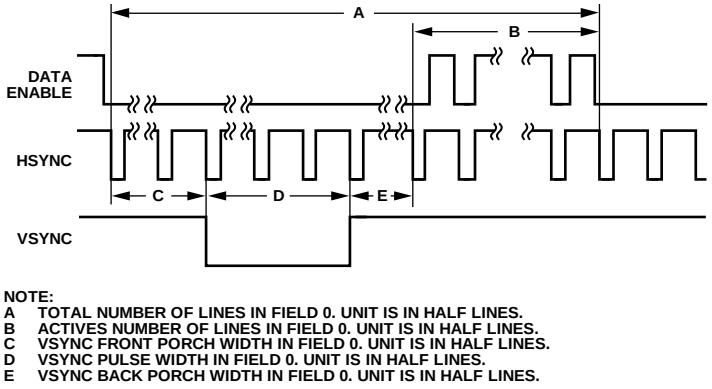


Figure 11. Vertical Parameters for FIELD 0

Note that Field 1 measurements must not be used for progressive video modes.

FIELD1_TOTAL_HEIGHT[13:0], Address 68 (HDMI), Address 0x28[5:0]; Address 0x29[7:0] (Read Only)

Field 1 total height is a vertical synchronization measurement. This readback gives the total number of half lines in Field 1. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1.

Table 86. FIELD1_TOTAL_HEIGHT[13:0] Function Description

FIELD1_TOTAL_HEIGHT[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in Field 1 (divide readback by 2 to get number of lines)

FIELD1_HEIGHT[12:0], Address 68 (HDMI), Address 0x0B[4:0]; Address 0x0C[7:0] (Read Only)

Field 1 height is a vertical filter measurement. This readback gives the number of active lines in field. This measurement is valid only when the vertical filter has locked. Field 1 measurements are only valid when HDMI_INTERLACED is set to 1.

Table 87. FIELD1_HEIGHT[12:0] Function Description

FIELD1_HEIGHT[12:0]	Description
xxxxxxxxxxxxx	The number of active lines in Field 1

FIELD1_VS_FRONT_PORCH[13:0], Address 68 (HDMI), Address 0x2C[5:0]; Address 0x2D[7:0] (Read Only)

Field 1 VSYNC front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1.

Table 88. FIELD1_VS_FRONT_PORCH[13:0] Function Description

FIELD1_VS_FRONT_PORCH[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in the VSYNC front porch of Field 1 (divide readback by 2 to get number of lines)

FIELD1_VS_PULSE_WIDTH[13:0], Address 68 (HDMI), Address 0x30[5:0]; Address 0x31[7:0] (Read Only)

Field 1 VSYNC width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1.

Table 89. FIELD1_VS_PULSE_WIDTH[13:0] Function Description

FIELD1_VS_PULSE_WIDTH[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in the VSYNC pulse of Field 1 (divide readback by 2 to get number of lines)

FIELD1_VS_BACK_PORCH[13:0], Address 68 (HDMI), Address 0x34[5:0]; Address 0x35[7:0] (Read Only)

Field 1 VSYNC back porch width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1.

Table 90. FIELD1_VS_BACK_PORCH[13:0] Function Description

FIELD1_VS_BACK_PORCH[13:0]	Description
xxxxxxxxxxxxx	The number of half lines in the VSYNC back porch of Field 1 (divide readback by 2 to get number of lines)

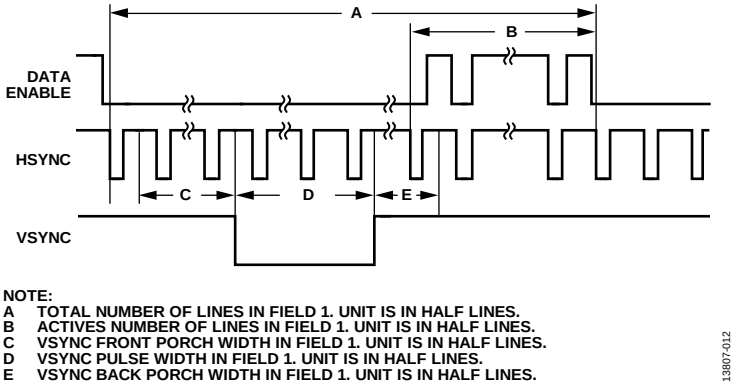


Figure 12. Vertical Parameters for Field 1

The vertical filter provides the interlaced status of the video stream. The interlaced status HDMI_INTERLACED is valid only if the vertical filter is locked and V_LOCKED_RAW is set to 1.

HDMI_INTERLACED, Address 68 (HDMI), Address 0x0B[5] (Read Only)

This bit is the HDMI input interlace status, a vertical filter measurement.

Table 91. HDMI_INTERLACED Function Description

HDMI_INTERLACED	Description
0	Progressive Input
1	Interlaced Input

Background Port Vertical Filter Measurements

The HDMI vertical filter performs the measurements described in this section on the HDMI port selected by BG_MEAS_PORT_SEL[2:0].

Note that BG_PARAM_LOCK must be high for background horizontal and vertical measurements to be valid.

BG_TOTAL_FIELD_HEIGHT[12:0], Address 68 (HDMI), Address 0xE8[4:0]; Address 0xE9[7:0] (Read Only)

Background port total field height is a vertical synchronization measurement for the background HDMI port determined by BG_MEAS_PORT_SEL[2:0]. The value represents the total number of lines in a field and is updated when an update request is made via the BG_MEAS_REQ control bit.

Table 92. BG_TOTAL_FIELD_HEIGHT[12:0] Function Description

BG_TOTAL_FIELD_HEIGHT[12:0]	Description
0000000000000	The total number of lines in a field on the background measurement port

BG_FIELD_HEIGHT[12:0], Address 68 (HDMI), Address 0xE6[4:0]; Address 0xE7[7:0] (Read Only)

Background port field height is a vertical synchronization measurement for a background HDMI port determined by BG_MEAS_PORT_SEL[2:0]. The value represents the number of active lines in a field and is updated when an update request is made via the BG_MEAS_REQ control bit.

Table 93. BG_FIELD_HEIGHT[12:0] Function Description

BG_FIELD_HEIGHT[12:0]	Description
0000000000000	The number of active lines in a Field on the background measurement port

BG_HDMI_INTERLACED, Address 68 (HDMI), Address 0xEA[0] (Read Only)

Background port HDMI input interlace status is a vertical filter measurement for a background HDMI port determined by BG_MEAS_PORT_SEL[2:0]. The status readback is updated when a update request is made via the BG_MEAS_REQ control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1.

Table 94. BG_HDMI_INTERLACED Function Description

BG_HDMI_INTERLACED	Description
0	Progressive Input
1	Interlaced Input

Vertical Filter Locking Mechanism

The HDMI vertical filter locks if the input VSYNC comes at exactly the same line count for two consecutive frames. The HDMI vertical filter unlocks if the VSYNC comes at a different pixels count for two consecutive frames.

Low Frequency Formats

To process the low frame rate video formats such as 720p24, 720p25, 720p30, 1080p23, 1080p24, and 1080p30, the NEW_VS_PARAM bit must be set (see Figure 13).

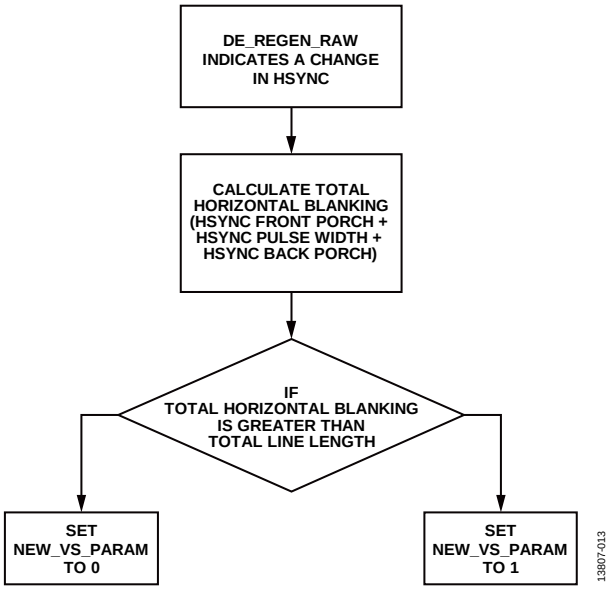


Figure 13. Low Frame Rate Algorithm

NEW_VS_PARAM, HDMI, Address 0x4C[2]

Enables a new version of vertical parameter extraction for evaluation purposes. That is the version in the background port measurement blocks.

Table 95. NEW_VS_PARAM Function Description

NEW_VS_PARAM	Description
0	NEW_VS_PARAM disabled
1	NEW_VS_PARAM enabled

AUDIO CONTROL AND CONFIGURATION

The ADV7613 extracts a pulse coded modulated (L-PCM), IEC 61937 compressed DSD, or HBR audio data stream from their corresponding audio packets (that is, audio sample, DSD, or HBR) encapsulated inside the HDMI data stream.

The ADV7613 also regenerates an audio master clock along with the extraction of the audio data. The clock regeneration is performed by an integrated DPLL. The regenerated clock is used to output audio data from the 64 stereo sample depth FIFO to the audio interface configuration pins.

Important

The ADV7613 supports the extraction of stereo audio data (noncompressed or compressed) at audio sampling frequency up to 192 kHz.

The ADV7613 supports the extraction of multichannel audio data.

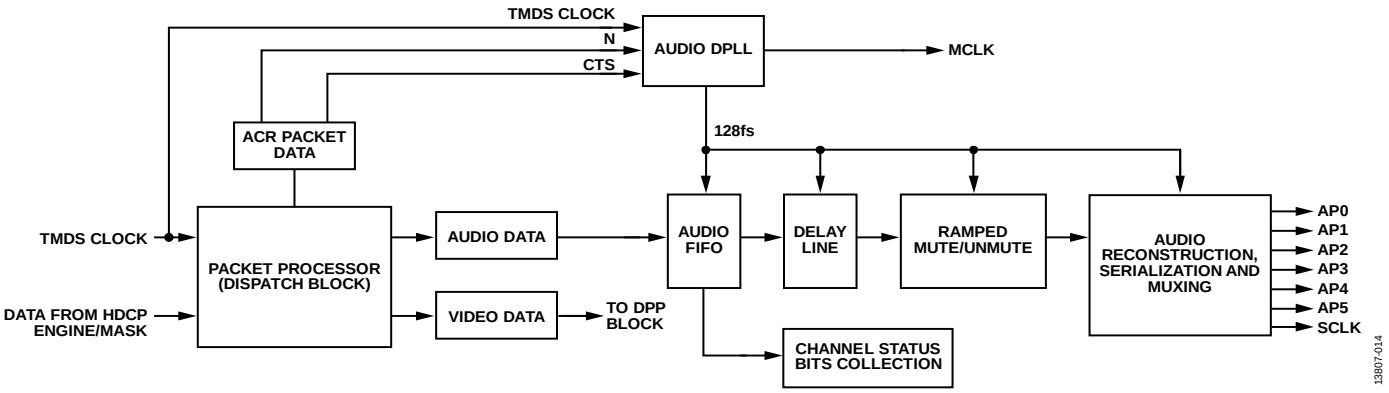


Figure 14. Audio Processor Block Diagram

Audio DPLL

The audio DPLL generates an internal audio master clock with a frequency of 128 times the audio sampling frequency, usually called f_S. The audio master clock is used to clock the audio processing section.

Locking Mechanism

When the upstream HDMI transmitter outputs a stable TMDS frequency and consistent audio clock regeneration values, the audio DPLL locks within two cycles of the audio master clock after the following two conditions are met:

- TMDS PLL is locked (see the TMDS_PLL_LOCKED description in Table 45)
- ADV7613 has received an ACR packet with N and CTS parameters within a valid range

The audio DPLL lock status can be monitored via AUDIO_PLL_LOCKED.

AUDIO_PLL_LOCKED, Address 68 (HDMI), Address 0x04[0] (Read Only)

A readback to indicate the Audio DPLL lock status.

Table 96. AUDIO_PLL_LOCKED Function Description

AUDIO_PLL_LOCKED	Description
0 (default)	The audio DPLL is not locked.
1	The audio DPLL is locked.

ACR Parameters Loading Method

The N and CTS parameters from the ACR packets are used to regenerate the audio clock and are reloaded into the DPLL anytime they change. The self clearing FORCE_N_UPDATE bit provides a means to reset the audio DPLL by forcing a reload of the N and CTS parameters from the ACR packet into the audio DPLL.

FORCE_N_UPDATE, Address 68 (HDMI), Address 0x5A[0] (Self Clearing)

FORCE_N_UPDATE is a control to force an N and CTS value update to the audio DPLL. The audio DPLL regenerates the audio clock.

Table 97. FORCE_N_UPDATE Function Description

FORCE_N_UPDATE	Description
0 (default)	No effect
1	Forces an update on the N and CTS values for audio clock regeneration

Audio DPLL Coast Feature

The audio DPLL incorporates a coast feature that allows it to indefinitely output a stable audio master clock when selectable events occur. The coast feature allows the audio DPLL to provide an audio master clock when the audio processor mutes the audio following a mute condition (see the Audio Muting section). The events that cause the audio DPLL to coast are selected via the coasts masks listed in Table 98.

Table 98. Selectable Coast Conditions

Bit Name	HDMI Map Address	Description	Corresponding Status Register(s)
AC_MSK_VCLK_CHNG	0x13[6]	When set to 1, audio DPLL coasts if TMDS clock has any irregular/missing pulses	VCLK_CHNG_RAW (see Table 221)
AC_MSK_VPLL_UNLOCK	0x13[5]	When set to 1, audio DPLL coasts if TMDS PLL unlocks	TMDS_PLL_LOCKED (see Table 45)
AC_MSK_NEW_CTS	0x13[3]	When set to 1, audio DPLL coasts if CTS changes by more than the threshold set in CTS_CHANGE_THRESHOLD[5:0] (see Table 150)	CTS_PASS_THRSH_RAW (see Table 149)
AC_MSK_NEW_N	0x13[2]	When set to 1, audio DPLL coasts if N changes	CHANGE_N_RAW (see Table 148)
AC_MSK_CHNG_PORT	0x13[1]	When set to 1, audio DPLL coasts if active port is changed	HDMI_PORT_SELECT (see Table 34)
AC_MSK_VCLK_DET	0x13[0]	When set to 1, audio DPLL coasts if no TMDS clock is detected on the active port	TMDS_CLK_A_RAW (see Table 35)

AUDIO FIFO

The audio FIFO can store up to 128 audio stereo data from the audio sample, DSD or HBR packets. Stereo audio data are added into the FIFO from the audio packet received. Stereo audio data are retrieved from the FIFO at a rate corresponding to 128 times the audio sampling frequency, f_S.

The status of the audio FIFO can be monitored through the following status flags: FIFO_UNDERFLO_RAW, FIFO_OVERFLO_RAW, FIFO_NEAR_OVFL_RAW, and FIFO_NEAR_UFLO_RAW.

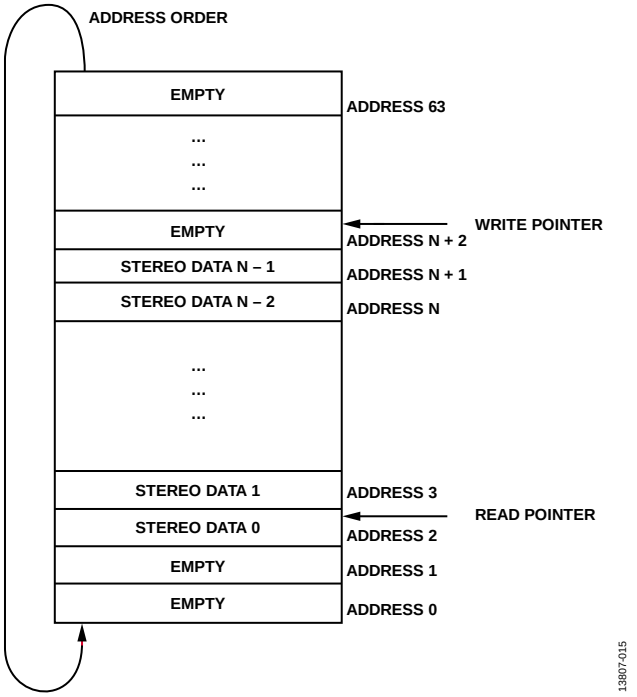


Figure 15. Audio FIFO

FIFO_UNDERFLO_RAW, IO, Address 0x7E[6] (Read Only)

FIFO_UNDERFLO_RAW is the status of audio FIFO underflow interrupt signal. When set to 1, it indicates the audio FIFO read pointer has reached the write pointer causing the audio FIFO to underflow. Once set, this bit remains high until it is cleared via AUDIO_FIFO_UNDERFLO_CLR.

Table 99. FIFO_UNDERFLO_RAW Function Description

FIFO_UNDERFLO_RAW	Description
0 (default)	Audio FIFO has not underflowed.
1	Audio FIFO has underflowed.

FIFO_OVERFLO_RAW, IO, Address 0x7E[5] (Read Only)

FIFO_OVERFLO_RAW is the status of audio FIFO overflow interrupt signal. When set to 1, it indicates audio FIFO write pointer has reached the read pointer causing the audio FIFO to overflow. Once set, this bit remains high until it is cleared via AUDIO_FIFO_OVERFLO_CLR.

Table 100. FIFO_OVERFLO_RAW Function Description

FIFO_OVERFLO_RAW	Description
0 (default)	Audio FIFO has not overflowed.
1	Audio FIFO has overflowed.

FIFO_NEAR_UFLO_RAW, IO, Address 0x83[0] (Read Only)

FIFO_NEAR_UFLO_RAW is the status of audio FIFO near underflow interrupt signal. When set to 1, it indicates the audio FIFO is near underflow as the number of FIFO registers containing stereo data is less or equal to value set in AUDIO_FIFO_ALMOST_EMPTY_ THRESHOLD. Once set, this bit remains high until it is cleared via FIFO_NEAR_UFLO_CLR.

Table 101. FIFO_NEAR_UFLO_RAW Function Description

FIFO_NEAR_UFLO_RAW	Description
0 (default)	Audio FIFO has not reached low threshold defined in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD [5:0].
1	Audio FIFO has reached low threshold defined in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD [5:0].

FIFO_NEAR_OVFL_RAW, IO, Address 0x7E[7] (Read Only)

FIFO_NEAR_OVFL_RAW is the status of audio FIFO near overflow interrupt signal. When set to 1, it indicates the audio FIFO is near overflow as the number FIFO registers containing stereo data is greater or equal to value set in AUDIO_FIFO_ALMOST_FULL_ THRESHOLD. Once set, this bit remains high until it is cleared via FIFO_NEAR_OVFL_CLR.

Table 102. FIFO_NEAR_OVFL_RAW Function Description

FIFO_NEAR_OVFL_RAW	Description
0 (default)	Audio FIFO has not reached high threshold defined in AUDIO_FIFO_ALMOST_FULL_THRESHOLD [5:0]
1	Audio FIFO has reached high threshold defined in AUDIO_FIFO_ALMOST_FULL_THRESHOLD [5:0]

AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6:0], Address 68 (HDMI), Address 0x12[6:0]

This bitfield sets the threshold used for FIFO_NEAR_UFLO_RAW. The FIFO_NEAR_UFLO_ST interrupt is triggered if audio FIFO goes below this level.

Table 103. AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6:0] Function Description

AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6:0]	Description
0x02 (default)	Default value

AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6:0], Address 68 (HDMI), Address 0x11[6:0]

This bitfield ets the threshold used for FIFO_NEAR_OVRFL_RAW. FIFO_NEAR_OVRFL_ST interrupt is triggered if audio FIFO reaches this level.

Table 104. AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6:0] Function Description

AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6:0]	Description
0x7D (default)	Default value

AUDIO PACKET TYPE FLAGS

The ADV7613 can receive the following audio packets:

- Audio sample packets (receive and process)
- HBR packets (receive and process)
- DSD packets (receive and process)
- DST packets (detection only)

The following flags are provided to monitor the type of audio packets received by the ADV7613. Figure 16 shows the algorithm that can be implemented to monitor the type of audio packet processed by the ADV7613.

AUDIO_MODE_CHNG_RAW, IO, Address 0x83[5] (Read Only)

This bit is the status of audio mode change interrupt signal. When set to 1, it indicates that the type of audio packet received has changed. The following are considered audio modes, no audio packets, audio sample packet, DSD packet, HBR packet or DST packet. Once set, this bit remains high until it is cleared via AUDIO_MODE_CHNG_CLR.

Table 105. AUDIO_MODE_CHNG_RAW Function Description

AUDIO_MODE_CHNG_RAW	Description
0 (default)	Audio mode has not changed.
1	Audio mode has changed.

AUDIO_SAMPLE_PCKT_DET, Address 68 (HDMI), Address 0x18[0] (Read Only)

This is the audio sample packet detection bit. This bit resets to zero on the 11th HSYNC leading edge following an audio packet if a subsequent audio sample packet has not been received or if a DSD, DST, or HBR audio packet sample packet has been received.

Table 106. AUDIO_SAMPLE_PCKT_DET Function Description

AUDIO_SAMPLE_PCKT_DET	Description
0 (default)	No L_PCM or IEC 61937 compressed audio sample packet received within the last 10 HSYNCs
1	L_PCM or IEC 61937 compressed audio sample packet received within the last 10 HSYNCs

DSD_PACKET_DET, Address 68 (HDMI), Address 0x18[1] (Read Only)

This is the DSD audio packet detection bit. This bit resets to zero on the 11th HSYNC leading edge following a DSD packet or if an audio, DST, or HBR packet sample packet has been received or after an HDMI reset condition.

Table 107. DSD_PACKET_DET Function Description

DSD_PACKET_DET	Description
0 (default)	No DSD packet received within the last 10 HSYNCs
1	DSD packet received within the last 10 HSYNCs

DST_AUDIO_PCKT_DET, Address 68 (HDMI), Address 0x18[2] (Read Only)

This is the DST audio packet detection bit. This bit resets to zero on the 11th HSYNC leading edge following a DST packet if a subsequent DST has not been received. Or if an audio, DSD, or HBR packet sample packet has been received or after an HDMI reset condition.

Table 108. DST_AUDIO_PCKT_DET Function Description

DST_AUDIO_PCKT_DET	Description
0 (default)	No DST packet received within the last 10 HSYNCs
1	DST packet received within the last 10 HSYNCs

HBR_AUDIO_PCKT_DET, Address 68 (HDMI), Address 0x18[3] (Read Only)

This is the HBR packet detection bit. This bit resets to zero on the 11th HSYNC leading edge following an HBR packet if a subsequent HBR packet has not been detected. It also resets if an Audio, DSD or DST packet sample packet has been received and after an HDMI reset condition.

Table 109. HBR_AUDIO_PCKT_DET Function Description

HBR_AUDIO_PCKT_DET	Description
0 (default)	No HBR audio packet received within the last 10 HSYNCs
1	HBR audio packet received within the last 10 HSYNCs

Note that the ADV7613 processes only one type of audio packet at a time, and processes the latest type of audio packet that it received.

AUDIO_SAMPL_PCKT_DET, DSD_PACKET_DET, DST_AUDIO_PCKT_DET, and HBR_AUDIO_PCKT_DET are reset to 0 when a HDMI packet detect reset condition occurs.

A corresponding interrupt can be enabled for AUDIO_MODE_CHNG_RAW by setting the mask AUDIO_MODE_CHNG_MB1 or AUDIO_MODE_CHNG_MB2. See the Interrupts section for additional information on the interrupt feature.

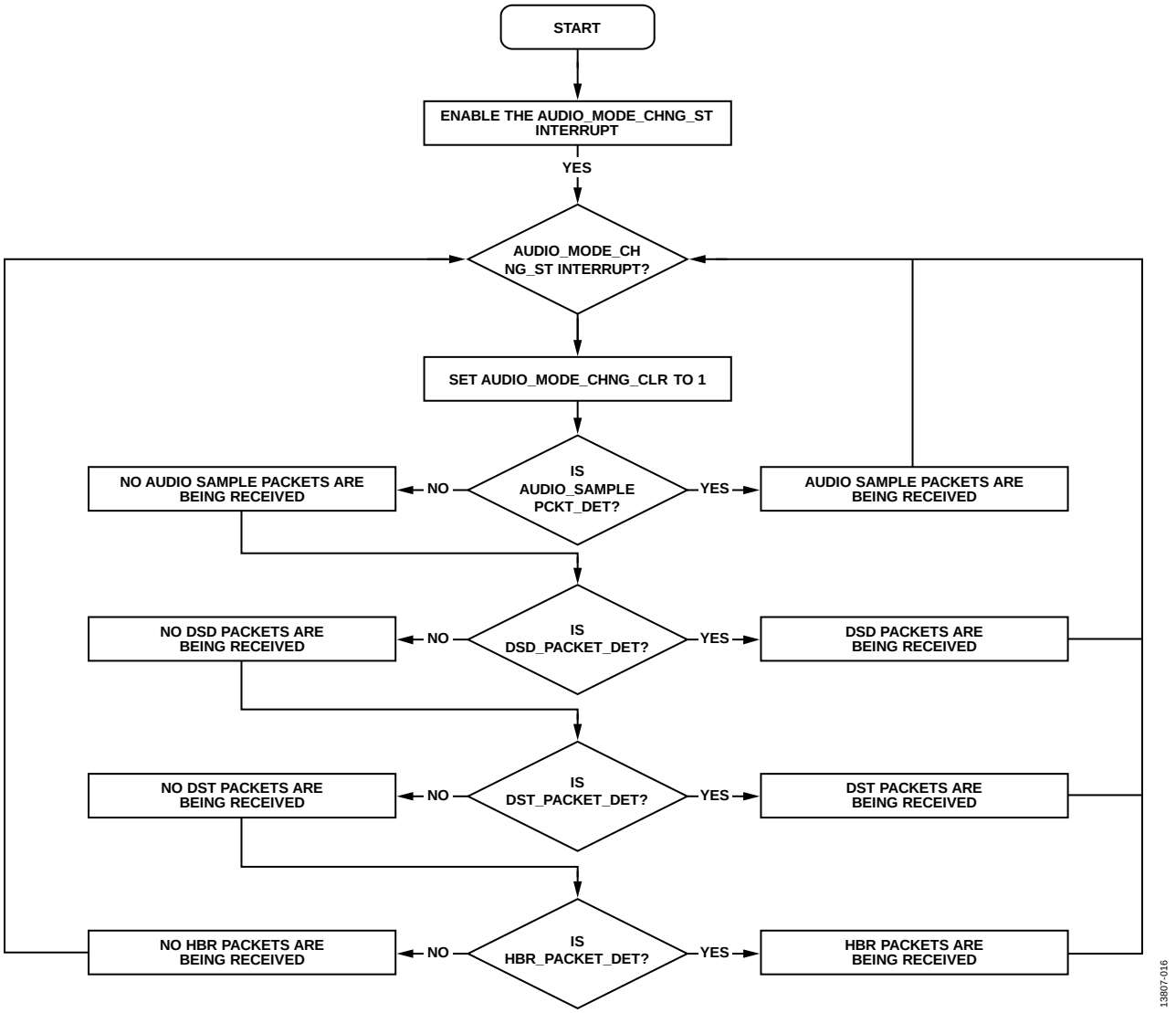


Figure 16. Monitoring Audio Packet Type Processed by ADV7613

AUDIO OUTPUT INTERFACE

The ADV7613 has a dedicated three-pin audio output interface. The output pin names and descriptions are shown in Table 110.

Table 110. Audio Outputs and Clocks

Output Pixel Port	Description
AP0	Audio Output Port 0
AP1	Audio Output Port 1
AP2	Audio Output Port 2
AP3	Audio Output Port 3
AP4	Audio Output Port 4
AP5	Audio Output Port 5
SCLK/INT2	Bit Clock
MCLK/INT2	Audio Master Clock

Table 111 shows the default configurations for the various possible output interfaces.

Table 111. Default Audio Output Pixel Port Mapping

Output Pixel Port	I²S/SPDIF Interface	DSD Interface
AP0	SPDIF0	DSD0A
AP1	I2S0/SDPIF0	DSD0B
AP2	I2S1/SDPIF1	DSD1A
AP3	I2S2/SDPIF2	DSD1B
AP4	I2S3/SDPIF3	DSD2A
AP5	LRCLK	DSD2B

Note that it is possible to tristate the audio pins using the global controls, as described in the Tristate Audio Output Drivers section. It is possible to output an AP0 signal (SPDIF0) to the AP1 pin using MUX_SPDIF_TO_I2S_ENABLE.

MUX_SPDIF_TO_I2S_ENABLE, Address 68 (HDMI), Address 0x6E[3]

This bit enables muxing SPDF data into the I²S pins (AP1).

Table 112. MUX_SPDIF_TO_I2S_ENABLE Function Description

MUX_SPDIF_TO_I2S_ENABLE	Description
0 (default)	Do not modify I²S outputs
1	Mux SPDIF into I²S pins

I²S/SPDIF Audio Interface and Output Controls

Two controls are provided to change the mapping between the audio output ports and the I²S and SPDIF (IEC60958) signals.

I2S_SPDIF_MAP_ROT[1:0], Address 68 (HDMI), Address 0x6D[5:4]

I2S_SPDIF_MAP_ROT[1:0] is a control to select the arrangement of the I²S/SPDIF interface on the audio output port pins.

Table 113. I2S_SPDIF_MAP_ROT[1:0] Function Description

I2S_SPDIF_MAP_ROT[1:0]	Description
00 (default)	I2S0/SPDIF0 on AP1 I2S1/SPDIF1 on AP2 I2S2/SPDIF2 on AP3 I2S3/SPDIF3 on AP4
01	I2S3/SPDIF3 on AP1 I2S0/SPDIF0 on AP2 I2S1/SPDIF1 on AP3 I2S2/SPDIF2 on AP4
10	I2S2/SPDIF2 on AP1 I2S3/SPDIF3 on AP2 I2S0/SPDIF0 on AP3 I2S1/SPDIF1 on AP4

I2S_SPDIF_MAP_ROT[1:0]	Description
11	I2S1/SPDIF1 on AP1 I2S2/SPDIF2 on AP2 I2S3/SPDIF3 on AP3 I2S0/SPDIF0 on AP4

I2S_SPDIF_MAP_INV, Address 68 (HDMI), Address 0x6D[6]

I2S_SPDIF_MAP_INV is a control to invert the arrangement of the I²S/SPDIF interface on the audio output port pins. Note that the arrangement of the I²S/SPDIF interface on the audio output port pins is determined by I2S_SPDIF_MAP_ROT.

Table 114. I2S_SPDIF_MAP_INV Function Description

I2S_SPDIF_MAP_INV	Description
0 (default)	Do not invert arrangement of I²S/SPDIF channels in audio output port pins
1	Invert arrangement of I²S/SPDIF channels in audio output port pins

I2S_SPDIF_MAP_ROT[1:0] and I2S_SPDIF_MAP_INV are independent controls. Any combination of values is therefore allowed for I2S_SPDIF_MAP_ROT[1:0] and I2S_SPDIF_MAP_INV. Table 115 and Table 116 show examples of mappings for the I2S/SPDIF signals.

Table 115. Audio Mappings for I2S_SPDIF_MAP_ROT = 00, I2S_SPDIF_MAP_INV = 0 (Default)

Output Audio Port	I²S/SPDIF Interface
AP1	I2S0/SDPIF0
AP2	I2S1/SDPIF1
AP3	I2S2/SDPIF2
AP4	I2S3/SDPIF3

Table 116. Audio Mappings for I2S_SPDIF_MAP_ROT = 00, I2S_SPDIF_MAP_INV = 1

Output Audio Port	I2S/SPDIF Interface
AP1	I2S3/SDPIF3
AP2	I2S2/SDPIF2
AP3	I2S1/SDPIF1
AP4	I2S0/SDPIF0

I2SBITWIDTH[4:0], Address 68 (HDMI), Address 0x03[4:0]

I2SBITWIDTH[4:0] is a control to adjust the bit width for right justified mode on the I²S interface.

Table 117. I2SBITWIDTH[4:0] Function Description

I2SBITWIDTH[4:0]	Description
00000	0 bit
00001	1 bit
00010	2 bits
…	…
11000 (default)	24 bits
11110	30 bits
11111	31 bits

I2SOUTMODE[1:0], Address 68 (HDMI), Address 0x03[6:5]

I2SOUTMODE[1:0] is a control to configure the I²S output interface.

Table 118. I2SOUTMODE[1:0] Function Description

I2SOUTMODE[1:0]	Description
00 (default)	I²S mode
01	Right justified
10	Left justified
11	Raw SPDIF (IEC60958) mode

I2SOUTMODE[1:0] is effective when the ADV7613 is configured to output I²S streams or AES3 streams, as in the following cases:

- The ADV7613 receives audio sample packets.
- The ADV7613 receives HBR packets, OVR_MUX_HBR is set to 1, and MUX_HBR_OUT is set to 2'b00, 2'b01, 2'b10, or 2'b11.
- In HBR mode, it is required that the part outputs four SPDIF, I²S, or raw IEC60958 streams encapsulating a 24-bit audio sample word. Therefore, I2SBITSWIDTH[4:0] must always be set to 0b11000.

The following audio formats can be output when the ADV7613 receives audio sample packets:

- Linear L-PCM audio data is output on the audio output pins if the part received audio sample packets with L-PCM encoded audio data. Each audio output pin carries stereo data that can be output in I²S, right justified, or left justified mode (see Figure 17, Figure 18, and Figure 19). The I2SOUTMODE[1:0] control must be set to 0x0, 0x01, or 0x2 to output I²S, right justified, and left justified respectively on the audio output pins.
- A stream conforming to the IEC60958 specification when the part receives audio sample packets with L-PCM encoded data (see Figure 20).
- An AES3 stream if the I2SOUTMODE[1:0] control is set to 0x3 (see Figure 21 and Figure 22). Note that AES3 is also referred to as raw SPDIF. Each AES3 stream may encapsulate stereo L-PCM audio data or multichannel non L-PCM audio data (for example, 5.1 Dolby Digital).
- Binary stream on the audio output pins when the part receives audio sample packets with non L-PCM encoded audio data (that is, AC-3 compressed audio) and if the following configuration is used:
  - I2SOUTMODE must be set to 0x0, 0x01, or 0x2 for I²S, right justified, and left justified format, respectively (see Figure 17, Figure 18, and Figure 19).
  - MT_MSK_COMPRS_AUD is set to 0.
  - Note that no audio flags are output by the part in that configuration. Each binary stream output by the part may encapsulate stereo L-PCM audio data or multichannel non L-PCM audio data (for example, 5.1 Dolby Digital).
- A stream conforming to the IEC61937 specification when the part receives audio sample packets with non L-PCM encoded audio data (for example, AC-3 compressed audio). The audio outputs can carry an audio stream that may be stereo or multichannel audio (for example, 5.1 Dolby Digital).

Table 119. I²S/SPDIF Interface Description

I²S/SPDIF Interface IO	Function
SPDIF0	SPDIF audio output
I2S0/SPDIF0	I²S audio (Channel 1, Channel 2)/SPDIF0
I2S1/SPDIF1	I²S audio (Channel 3, Channel 4)/SPDIF1
I2S2/SPDIF2	I²S audio (Channel 5, Channel 6)/SPDIF2
I2S3/SPDIF3	I²S audio (Channel 7, Channel 8)/SPDIF3
SCLK	Bit clock
LRCLK	Data output clock for left and right channel
MCLKOUT	Audio master clock output

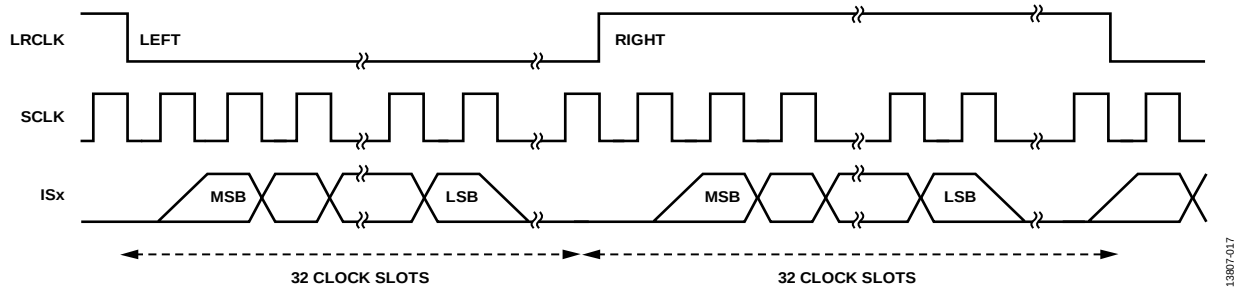


Figure 17. Timing Audio Data Output in I²S Mode

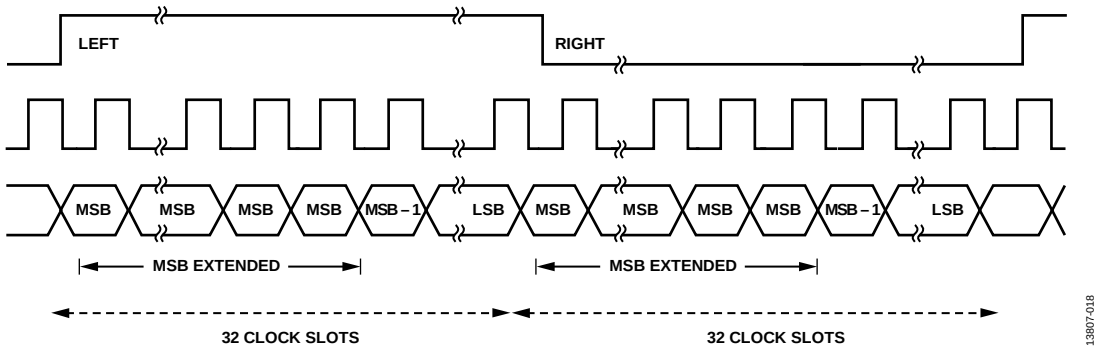


Figure 18. Timing Audio Data Output in Right Justified Mode

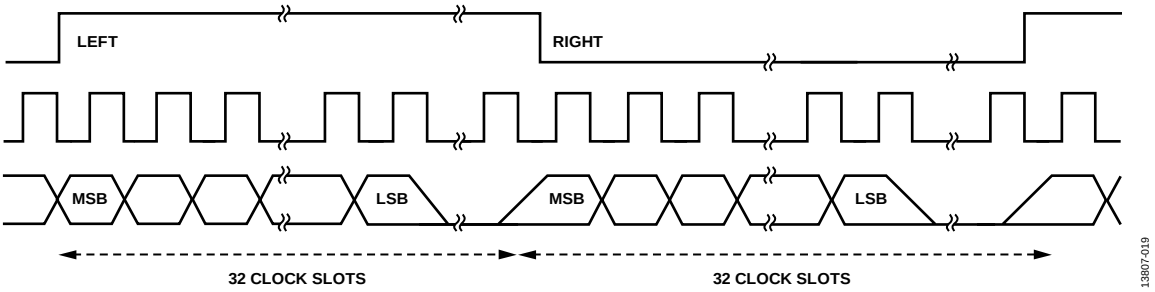


Figure 19. Timing Audio Data Output in Left Justified Mode

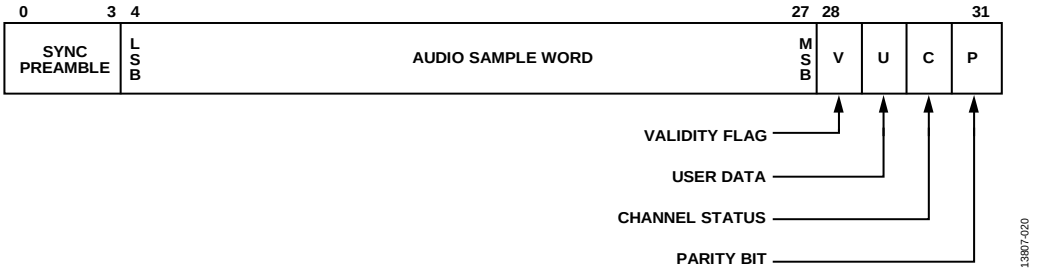


Figure 20. IEC 60958 Subframe Timing Diagram

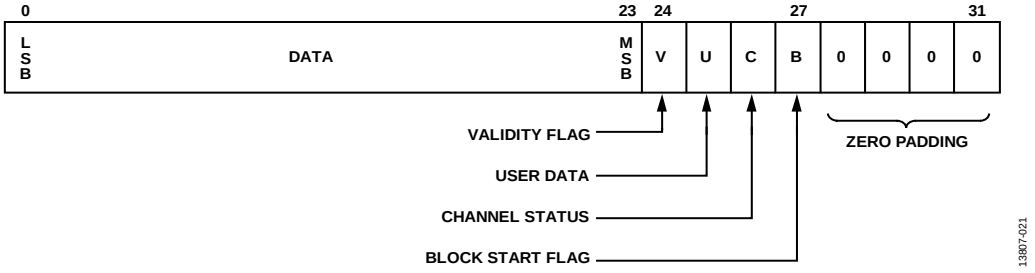


Figure 21. AES3 Subframe Timing Diagram

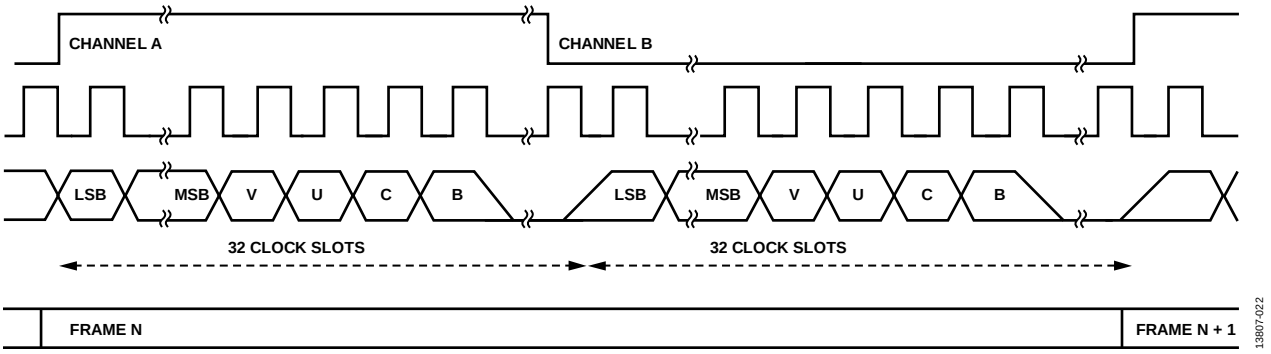


Figure 22. AES3 Stream Timing Diagram

DSD Audio Interface and Output Controls

The ADV7613 incorporates a 6-DSD channel interface used to output the audio stream extracted from DSD packets. Each of the DSD channels carries an oversampled 1-bit representation of the audio signal as delivered on super audio CDs (SACDs).

Table 120. DSD Interface Description

DSD Interface IO	Function
DSD0A	First DSD data channel
DSD0B	Second DSD data channel
DSD1A	Third DSD data channel
DSD1B	Fourth DSD data channel
DSD2A	Fifth DSD data channel
DSD2B	Sixth DSD data channel
SCLK	Bit clock
MCLKOUT	Audio master clock output

Two controls are provided to change the mapping between the audio output ports and DSD signals.

DSD_MAP_ROT[2:0], Address 68 (HDMI), Address 0x6D[2:0]

DSD_MAP_ROT[2:0] is a control to select the arrangement of the DSD interface on the audio output port pins.

Table 121. DSD_MAP_ROT[2:0] Function Description

DSD_MAP_ROT[2:0]	Description
000 (default)	DSD0A on AP0 DSD0B on AP1 DSD1A on AP2 DSD1B on AP3 DSD2A on AP4 DSD2B on AP5
001	DSD2B on AP0 DSD0A on AP1 DSD0B on AP2 DSD1A on AP3 DSD1B on AP4 DSD2A on AP5
010	DSD2A on AP0 DSD2B on AP1 DSD0A on AP2 DSD0B on AP3 DSD1A on AP4 DSD1B on AP5

DSD_MAP_ROT[2:0]	Description
011	DSD1B on AP0 DSD2A on AP1 DSD2B on AP2 DSD0A on AP3 DSD0B on AP4 DSD1A on AP5
100	DSD1A on AP0 DSD1B on AP1 DSD2A on AP2 DSD2B on AP3 DSD0A on AP4 DSD0B on AP5
101	DSD0B on AP0 DSD1A on AP1 DSD1B on AP2 DSD2A on AP3 DSD2B on AP4 DSD0A on AP5
110	Reserved
111	Reserved

DSD_MAP_INV, Address 68 (HDMI), Address 0x6D[3]

This bit is control to invert the arrangement of the DSD interface on the audio output port pins. Note the arrangement of the DSD interface on the audio output port pins is determined by DSD_MAP_ROT[2:0].

Table 122. DSD_MAP_INV Function Description

DSD_MAP_INV	Description
0 (default)	Do not invert arrangement of the DSD channels on the audio output port pins
1	Invert arrangement of the DSD channels on the audio output port pins

DSD_MAP_ROT[2:0]and DSD_MAP_INV are independent controls. Any combination of values is therefore allowed for DSD_MAP_ROT[2:0] and DSD_MAP_INV. Table 123 and Table 124 show examples of mappings for the DSD signals.

Table 123. Audio Mapping for DSD_MAP_ROT = 00, DSD_MAP_INV = 0 (Default)

Output Pixel Port Name	DSD Interface
AP0	DSD0A
AP1	DSD0B
AP2	DSD1A
AP3	DSD1B
AP4	DSD2A
AP5	DSD2B

Table 124. Audio Mapping for DSD_MAP_ROT = 00, DSD_MAP_INV = 1

Output Pixel Port Name	DSD Interface
AP0	DSD2B
AP1	DSD2A
AP2	DSD1B
AP3	DSD1A
AP4	DSD0B
AP5	DSD0A

Note that the DSD0A and DSD0B output must be used when in stereo mode only. DSD0A and DSD0B always carry the main two-channel audio data. DSD1A, DSD1B, DSD2A, and DSD2B are the surround channels.

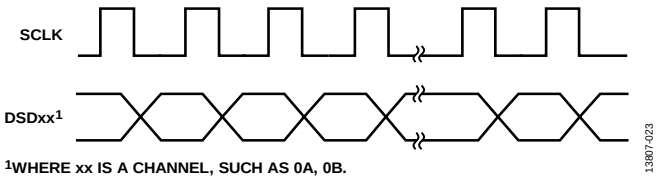


Figure 23. DSD Timing Diagram

By default, the ADV7613 automatically enables the DSD interface if it receives DSD packets. The ADV7613 also automatically enables the I²S interface if it receives audio sample packets or if it does not receive any audio packets. However, it is possible to override the audio interface that is used via the OVR_AUTO_MUX_DSD_OUT and MUX_DSD_OUT controls.

OVR_AUTO_MUX_DSD_OUT, Address 68 (HDMI), Address 0x01[3]

OVR_AUTO_MUX_DSD_OUT is the DSD/DST override control. In automatic control, DSD or I²S interface is selected according to the type of packet received. The DSD/DST interface is enabled if the device receives DSD or DST audio sample packet. The I²S interface is enabled when the device receives audio sample packets or when no packet is received. In manual mode, MUX_DSD_OUT selects the output interface.

Table 125. OVR_AUTO_MUX_DSD_OUT Function Description

Function

OVR_AUTO_MUX_DSD_OUT	Description
0 (default)	Automatic DSD/DST output control
1	Override DSD/DST output control

MUX_DSD_OUT, Address 68 (HDMI), Address 0x01[4]

MUX_DSD_OUT is an override control for the DSD output.

Table 126. MUX_DSD_OUT Function Description

Function

MUX_DSD_OUT	Description
0	Override by outputting I²S data
1	Override by outputting DSD/DST data

HBR Interface and Output Controls

The ADV7613 can receive HBR audio stream packets. The ADV7613 outputs HBR data over four of the audio output pins in any of the three following formats.

The ADV7613 can output HBR data as an SDPIF stream conforming to the IEC60958 specification (see Figure 20). One of the following configurations is required to output an SPDIF stream on the HBR output pins:

- OVR_MUX_HBR is set to 0.
- OVR_MUX_HBR is set to 1 and MUX_HBR_OUT is set to 1.

The ADV7613 can output HBR data as a binary stream, if one of the following configurations is used (note that no audio flags are output by the device in these configurations):

- OVR_MUX_HBR is set to 1, MUX_HBR_OUT is set to 0, and I2SOUTMODE[1:0] is set to 0x0 for an I²S mode binary stream (see Figure 17).
- OVR_MUX_HBR is set to 1, MUX_HBR_OUT is set to 0, and I2SOUTMODE[1:0] is set to 0x1 for a right justified stream (see Figure 18).
- OVR_MUX_HBR is set to 1, MUX_HBR_OUT is set to 0, and I2SOUTMODE[1:0] is set to 0x2 for a left justified stream (see Figure 19).

The ADV7613 can output HBR data as an AES3 stream on each HBR interface output pin (see Figure 21 and Figure 22). The following configuration is required to output AES3 streams:

- OVR_MUX_HBR is set to 1.
- I2SOUTMODE[1:0] is set to 0b11.

It is important to note that each of the four HBR outputs carry one of four consecutive blocks of the HBR stream, and the four streams on the four HBR pin are output at one quarter of the audio sample rate, f_S.

Table 127. HBR Interface Description

HBR Interface IO	Function
AP1	First block of HBR stream.
AP2	Second block of HBR stream
AP3	Third block of HBR stream
AP4	Fourth block of HBR stream
SCLK	Bit clock
LRCLK	Data output clock for left and right channel
MCLKOUT	Audio master clock output

Note that the audio output mapping controls, I2S_SPDIF_MAP_ROT[1:0] and I2S_SPDIF_MAP_INV, also apply to the HBR output signals. Also note that the audio output interface pin AP0 also carries the SPDIF0 output, regardless of I2S_SPDIF_MAP_ROT[1:0] and I2S_SPDIF_MAP_INV.

OVR_MUX_HBR, Address 68 (HDMI), Address 0x01[2]

OVR_MUX_HBR is a control to select automatic or manual configuration for HBR outputs. HBR outputs are automatically encoded as SPDIF streams. In manual mode, MUX_HBR_OUT selects the audio output interface.

Table 128. OVR_MUX_HBR Function Description

OVR_MUX_HBR	Description
0 (default)	Automatic HBR output control
1	Manual HBR output control

MUX_HBR_OUT, Address 68 (HDMI), Address 0x01[1]

MUX_HBR_OUT is a control to manually select the audio output interface for HBR data. It is valid when OVR_MUX_HBR is set to 1.

Table 129. MUX_HBR_OUT Function Description

MUX_HBR_OUT	Description
0 (default)	Override by outputting I^2S data
1	Override by outputting SPDIF data

MCLKOUT SETTING

The frequency of audio master clock MCLKOUT is set using the MCLK_FS_N[2:0] register, as shown in Equation 3, in the relationship between MCLKOUT, MCLKFS_N, and f_S.

$$MCLKOUT = (MCLKFS\_N[2:0] + 1) \times 128 \times f_S \quad (3)$$

MCLK_FS_N[2:0], Address 4C (DPLL), Address 0xB5[2:0]

MCLK_FS_N[2:0] selects the frequency of MCLK out as multiple of 128 f_S.

Table 130. MCLK_FS_N[2:0] Function Description

MCLK_FS_N[2:0]	Description
000	128 f_S
001 (default)	256 f_S
010	384 f_S
011	512 f_S
100	640 f_S
101	768 f_S
110	Not valid
111	Not valid

AUDIO CHANNEL MODE

AUDIO_CH_MD_RAW indicates if 2-channel audio data or multichannel audio data is received.

AUDIO_CH_MD_RAW, IO, Address 0x65[4] (Read Only)

This bit is the raw status signal indicating the layout value of the audio packets that were last received.

Table 131. AUDIO_CH_MD_RAW Function Description

AUDIO_CH_MD_RAW	Description
0	The last audio packets received have a layout value of 1. (For example, Layout 1 corresponds to 2-channel audio when audio sample packets are received.)
1	The last audio packets received have a layout value of 0. (For example, Layout 0 corresponds to 8-channel audio when audio sample packets are received.)

Note that the audio CH_MD_RAW flag is valid for audio sample packets and DSD packets.

AUDIO_CHANNEL_MODE, Address 68 (HDMI), Address 0x07[6] (Read Only)

This bit flags stereo or multichannel audio packets. Note that stereo packets can carry compressed multichannel audio.

Table 132. AUDIO_CHANNEL_MODE Function Description

AUDIO_CHANNEL_MODE	Description
0	Stereo audio (may be compressed multichannel)
1	Multichannel uncompressed audio detected (Channel 3 to Channel 8).

AUDIO MUTING

The ADV7613 integrates an advanced audio mute function that is designed to remove all extraneous noise and pops from a 2-channel L-PCM audio stream at sample frequencies up to 48 kHz.

The hardware for audio mute function is composed of the following three blocks:

- Audio delay line that delays Channel 1 and Channel 2 by 512 stereo samples.
- Audio mute controller takes in event detection signals that can be used to determine when an audio mute is needed. The controller generates a mute signal to the ramped audio block and a coast signal to the digital PLL generating the audio clock.
- Ramped audio mute block that can mute the audio over the course of 512 stereo samples.

Note that the ADV7613 mutes only the noncompressed data from the audio sample packets output through the I^2S and the SPDIF interface.

The audio delay line is automatically bypassed when the ADV7613 receives multichannel audio or when it receives DSD packets or HBR packets. The ramped audio mute block is always bypassed when the device receives compressed audio or when it receives DSD packets or HBR packets.

Delay Line Control

The audio delay line must be enabled when the ADV7613 is configured for automatic mute. The audio delay line is controlled by the MAN_AUDIO_DL_BYPASS and AUDIO_DELAY_LINE_BYPASS bits.

MAN_AUDIO_DL_BYPASS, Address 68 (HDMI), Address 0x0F[7]

This bit is the audio delay bypass manual enable. The audio delay line is automatically active for stereo samples and bypassed for multichannel samples. By setting MAN_AUDIO_DL_BYPASS to 1, the audio delay bypass configuration can be set by the user with the AUDIO_DELAY_LINE_BYPASS control.

Table 133. MAN_AUDIO_DL_BYPASS Function Description

MAN_AUDIO_DL_BYPASS	Description
0 (default)	Audio delay line is automatically bypassed if multichannel audio is received. The audio delay line is automatically enabled if stereo audio is received.
1	Overrides automatic bypass of audio delay line. Audio delay line is applied depending on the AUDIO_DELAY_LINE_BYPASS control.

AUDIO_DELAY_LINE_BYPASS, Address 68 (HDMI), Address 0x0F[6]

This bit is the manual bypass control for the audio delay line. It is only valid if MAN_AUDIO_DL_BYPASS is set to 1.

Table 134. AUDIO_DELAY_LINE_BYPASS Function Description

AUDIO_DELAY_LINE_BYPASS	Description
0 (default)	Enables the audio delay line
1	Bypasses the audio delay line

Audio Mute Configuration

The ADV7613 can be configured to automatically mute an L-PCM audio stream when selectable mute conditions occur. Configure the audio muting as follows:

- Set the audio muting speed via AUDIO_MUTE_SPEED[4:0].
- Set NOT_AUTO_UNMUTE as follows:
  - Set NOT_AUDIO_UNMUTE[2:0] to 0 if the audio must be unmuted automatically after a delay set in WAIT_UNMUTE[2:0] after all selected mute conditions have become inactive.
  - Set NOT_AUTO_UNMUTE to 1 if the audio must be unmuted manually (for example, by an external controller) when all selected mute conditions have become inactive.
  - Select the mute conditions that trigger an audio mute (see Table 139).
- Select the Audio PLL coast conditions (see the Audio DPLL Coast Feature section).
- Set WAIT_UNMUTE[2:0] to configure the audio counter that triggers the audio unmute when it has timed out after all selected mute conditions have become inactive.

The ADV7613 internally unmutes the audio if the following three conditions (listed in order of priority) are met:

- Mute conditions are inactive.
- NOT_AUTO_UNMUTE is set to 0.
- Audio unmute counter has finished counting down or is disabled.

Note that both Table 98 and Table 139 provide a column with the heading, Corresponding Status Register(s). This column lists the status registers that convey information related to their corresponding audio mute masks or coast masks.

The ADV7613 also mutes the DSD stream when one of the selected mute conditions occurs (see Table 139) by outputting the DSD mute pattern 0101010101… A DSD decoder receiving this stream outputs a 0 V mean analog stream.

The ADV7613 can mute the audio data with compressed audio data or HBR packets. In these cases, mute outputs a constant stream of 0.

For the best audio muting performance, it is recommended to set AUDIO_MUTE_SPEED to 1 when the ADV7613 receives multichannel sample packets.

For best audio muting performance, the following settings are recommended when the audio sampling frequency of the audio stream is greater than 48 kHz:

- Set AUDIO_MUTE_SPEED to 1
- Set MAN_AUDIO_DL_BYPASS to 1
- Set AUDIO_DELAY_LINE_BYPASS to 1

For best audio muting performance, the following settings are recommended when the audio sampling frequency of the audio stream is equal to or lower than 48 kHz:

- Set AUDIO_MUTE_SPEED to 0x1F
- Set MAN_AUDIO_DL_BYPASS to 0

MUTE_AUDIO, Address 68 (HDMI), Address 0x1A[4]

MUTE_AUDIO is a control to force an internal mute independently of the mute mask conditions.

Table 135. MUTE_AUDIO Function Description

MUTE_AUDIO	Description
0 (default)	Audio in normal operation
1	Force audio mute

AUDIO_MUTE_SPEED[4:0], Address 68 (HDMI), Address 0x0F[4:0]

AUDIO_MUTE_SPEED[4:0] is the number of samples between each volume change of 1.5 dB when muting and unmuting.

Table 136. AUDIO_MUTE_SPEED[4:0] Function Description

AUDIO_MUTE_SPEED[4:0]	Description
0x1F (default)	Default value

NOT_AUTO_UNMUTE, Address 68 (HDMI), Address 0x1A[0]

NOT_AUTO_UNMUTE is a control to disable the automatic unmute feature. When set to 1, audio can be unmuted manually if all mute conditions are inactive by setting NOT_AUTO_UNMUTE to 0 and then back to 1.

Table 137. NOT_AUTO_UNMUTE Function Description

NOT_AUTO_UNMUTE	Description
0 (default)	Audio unmutes following a delay set by WAIT_UNMUTE after all mute conditions have become inactive
1	Prevents audio from unmuting automatically

WAIT_UNMUTE[2:0], Address 68 (HDMI), Address 0x1A[3:1]

WAIT_UNMUTE[2:0] is a control to delay audio unmute. Once all mute conditions are inactive, WAIT_UNMUTE[2:0] can specify a further delay time before unmuting. NOT_AUTO_UNMUTE must be set to 0 for this control to be effective.

Table 138. WAIT_UNMUTE[2:0] Function Description

WAIT_UNMUTE[2:0]	Description
000 (default)	Disables/cancels delayed unmute. Audio unmutes directly after all mute conditions become inactive.
001	Unmutes 250 ms after all mute conditions become inactive.
010	Unmutes 500 ms after all mute conditions become inactive.
011	Unmutes 750 ms after all mute conditions become inactive.
100	Unmutes 1 sec after all mute conditions become inactive.

Table 139. Selectable Mute Conditions

Bit Name	HDMI Map Address	Description	Corresponding Status Register(s)
MT_MSK_COMPRS_AUD	0x14[5]	Causes audio mute if audio is compressed	CS_DATA[1]
MT_MSK_AUD_MODE_CHNG	0x14[4]	Causes audio mute if audio mode changes between PCM, DSD, DST, or HBR formats	AUDIO_SAMPLE_PCKT_DET
MT_MSK_PARITY_ERR	0x14[1]	Causes audio mute if parity bits in audio samples are not correct	PARITY_ERROR_RAW
MT_MSK_VCLK_CHNG	0x14[0]	Causes audio mute if TMDS clock has irregular/missing pulses	VCLK_CHNG_RAW
MT_MSK_APLL_UNLOCK	0x15[7]	Causes audio mute if audio PLL unlocks	AUDIO_PLL_LOCKED
MT_MSK_VPLL_UNLOCK	0x15[6]	Causes audio mute if TMDS PLL unlocks	TMDS_PLL_LOCKED
MT_MSK_ACR_NOT_DET	0x15[5]	Causes audio mute if ACR packets are not received within one VSYNC	AUDIO_C_PCKT_RAW
MT_MSK_FLATLINE_DET	0x15[3]	Causes audio mute if flatline bit in audio packets is set	AUDIO_FLT_LINE_RAW
MT_MSK_FIFO_UNDERFLOW	0x15[1]	Causes audio mute if audio FIFO underflows	FIFO_UNDERFLO_RAW
MT_MSK_FIFO_OVERFLOW	0x15[0]	Causes audio mute if audio FIFO overflows	FIFO_OVERFLO_RAW
MT_MSK_AVMUTE	0x16[7]	Causes audio mute if AVMUTE is set in the general control packet	AV_MUTE_RAW
MT_MSK_NOT_HDMIMODE	0x16[6]	Causes audio mute if HDMI_MODE bit goes low	HDMI_MODE
MT_MSK_NEW_CTS	0x16[5]	Causes audio mute if CTS changes by more than the threshold set in CTS_CHANGE_THRESHOLD[5:0]	CTS_PASS_THRSH_RAW
MT_MSK_NEW_N	0x16[4]	Causes audio mute if N changes	CHANGE_N_RAW
MT_MSK_CHMODE_CHNG	0x16[3]	Causes audio mute if the channel mode changes from stereo to multichannel, or vice versa	AUDIO_MODE_CHNG_RAW
MT_MSK_APCKT_ECC_ERR	0x16[2]	Causes audio mute if uncorrectable error is detected in the audio packets by the ECC block	AUDIO_PCKT_ERR_RAW

Bit Name	HDMI Map Address	Description	Corresponding Status Register(s)
MT_MSK_CHNG_PORT	0x16[1]	Causes audio mute if HDMI port is changed	HDMI_PORT_SELECT
MT_MSK_VCLK_DET	0x16[0]	Causes audio mute if TMDS clock is not detected	TMDS_CLK_A_RAW

Internal Mute Status

The internal mute status is provided through the INTERNAL_MUTE_RAW bit.

INTERNAL_MUTE_RAW, IO, Address 0x65[6] (Read Only)

This bit is the raw status signal of internal mute signal.

Table 140. INTERNAL_MUTE_RAW Function Description

INTERNAL_MUTE_RAW	Description
0 (default)	Audio is not muted
1	Audio is muted

AV Mute Status

AV_MUTE, Address 68 (HDMI), Address 0x04[6] (Read Only)

This bit is the readback of the AVMUTE status received in the last general control packet received.

Table 141. AV_MUTE Function Description

AV_MUTE	Description
0 (default)	AVMUTE not set
1	AVMUTE set

Audio Mute Signal

The ADV7613 can output an audio mute signal that can be used to control the muting in a back end audio device processing the audio data output by the ADV7613 (for example, DSP).

The audio mute signal is output on the INT1 pin by setting EN_UMASK_RAW_INTRQ to 1. The mute signal is active high.

It is important to note that the ADV7613 may interface with an audio processor (for example, DSP) in which the muting of the audio is implemented. In this case, the audio processor typically features a delay line followed by a mute block for audio mute and unmuting purposes. The following hardware and software configuration is recommended for optimum muting performance of the ADV7613 and audio processor system:

- Connect the mute signal of the ADV7613 to the audio processor mute input. The ADV7613 mute signal can now drive the muting/unmuting of the audio data inside the audio processor.
- Bypass the audio delay line of the ADV7613 with the following settings:
  - Set MAN_AUDIO_DL_BYPASS to 1.
  - Set AUDIO_DELAY_LINE_BYPASS to 1.
  - Configure the ADV7613 to mute the audio over one audio sample clock. Set AUDIO_MUTE_SPEED[4:0] to 1, which ensures that the ADV7613 never outputs invalid audio data out to the audio processor.

EN_UMASK_RAW_INTRQ, IO Map, Address 0x40[3]

This bit is a control to apply the audio mute signal on INT1 interrupt pin.

Table 142. EN_UMASK_RAW_INTRQ Function Description

EN_UMASK_OUT_INTRQ	Description
0 (default)	Does not output raw interrupt flag on INT1
1	Outputs raw interrupt flag on INT1

Audio Stream with Incorrect Parity Error

The ADV7613 discards audio sample packets that have an incorrect parity bit. When these samples are received, the ADV7613 repeats the previous audio sample with a valid parity bit. The audio stream out of the ADV7613 can be muted in this situation if the audio mute mask MT_MSK_PARITY_ERR is set.

It is possible to configure the ADV7613 so that it processes audio sample packets that have an incorrect parity bit and corrects the parity bit. The ADV7613 can then output an audio stream even when the parity bits from the audio sample packet are invalid. This configuration is activated by setting MT_MSK_PARITY_ERR 0 and IGNORE_PARITY_ERR to 1.

IGNORE_PARITY_ERR, Address 68 (HDMI), Address 0x1A[6]

This bit is a control to select the processing of audio samples even when they have a parity error.

Table 143. IGNORE_PARITY_ERR Function Description

IGNORE_PARITY_ERR	Description
0 (default)	Discard audio sample packets that have an invalid parity bit
1	Process audio sample packets that have an invalid parity bit

MT_MSK_PARITY_ERR, Address 68 (HDMI), Address 0x14[1]

MT_MSK_PARITY_ERR is the audio mute mask for a parity error. It sets the audio mutes if an audio sample packet is received with an incorrect parity bit.

Table 144. MT_MSK_PARITY_ERR Function Description

MT_MSK_PARITY_ERR	Description
1 (default)	Audio mute occurs if an audio sample packet is received with an incorrect parity bit

AUDIO CLOCK REGENERATION PARAMETERS

The ADV7613 recreates an internal audio master clock using audio clock regeneration (ACR) values transmitted by the HDMI source.

ACR Parameters Readbacks

The N and CTS registers can be read back from the HDMI map.

CTS[19:0], Address 68 (HDMI), Address 0x5B[7:0]; Address 0x5C[7:0]; Address 0x5D[7:4] (Read Only)

CTS[19:0] is a readback for the CTS value received in the HDMI data stream.

Table 145. CTS[19:0] Function Description

CTS[19:0]	Description
00000000000000000000 (default)	Default CTS value readback from HDMI stream
xxxxxxxxxxxxxxxxxxxx	CTS value readback from HDMI stream

N[19:0], Address 68 (HDMI), Address 0x5D[3:0]; Address 0x5E[7:0]; Address 0x5F[7:0] (Read Only)

N[19:0] is a readback for the N value received in the HDMI data stream.

Table 146. N[19:0] Function Description

N[19:0]	Description
00000000000000000000 (default)	Default N value readback from HDMI stream
xxxxxxxxxxxxxxxxxxxx	N value readback from HDMI stream

Note that a buffer is implemented for the N and CTS readback registers. After a read of the HDMI map, Address 0x5B updates the buffer that stores the N and CTS readback registers. The buffer implemented for N and CTS readback allows the reading of both the N and CTS registers within an I^2C block read.

Monitoring ACR Parameters

The reception of ACR packets can be notified via the AUDIO_C_PCKT_RAW flag. Changes in N and CTS can be monitored via the CHANGE_N_RAW and CTS_PASS_THRSH_RAW flags, as described in this section.

AUDIO_C_PCKT_RAW, IO, Address 0x65[1] (Read Only)

AUDIO_C_PCKT_RAW is the raw status signal of audio clock regeneration packet detection signal.

Table 147. AUDIO_C_PCKT_RAW Function Description

AUDIO_C_PCKT_RAW	Description
0 (default)	No audio clock regeneration packets received since the last HDMI reset condition
1	Audio clock regeneration packets received

CHANGE_N_RAW, IO, Address 0x7E[3] (Read Only)

CHANGE_N_RAW is the status of the ACR N value changed interrupt signal. When set to 1, it indicates that the N value of the ACR packets has changed. Once set, this bit remains high until it is cleared via CHANGE_N_CLR.

Table 148. CHANGE_N_RAW Function Description

CHANGE_N_RAW	Description
0 (default)	Audio clock regeneration N value has not changed.
1	Audio clock regeneration N value has changed.

CTS_PASS_THRSH_RAW, IO, Address 0x7E[4] (Read Only)

CTS_PASS_THRSH_RAW is the status of the ACR CTS value exceed threshold interrupt signal. When set to 1, it indicates that the CTS value of the ACR packets has exceeded the threshold set by CTS_CHANGE_THRESHOLD. Once set, this bit remains high until it is cleared via CTS_PASS_THRSH_CLR.

Table 149. CTS_PASS_THRSH_RAW Function Description

CTS_PASS_THRSH_RAW	Description
0 (default)	Audio clock regeneration CTS value has not passed the threshold.
1	Audio clock regeneration CTS value has changed more than threshold.

CTS_CHANGE_THRESHOLD[5:0], Address 68 (HDMI), Address 0x10[5:0]

CTS_CHANGE_THRESHOLD[5:0] sets the tolerance for change in the CTS value. This tolerance is used for the audio mute mask MT_MSK_NEW_CTS and the HDMI status bit CTS_PASS_THRSH_RAW and the HDMI interrupt status bit CTS_PASS_THRSH_ST. This register controls the amounts of LSBs that the CTS can change before an audio mute, status change, or interrupt is triggered.

Table 150. CTS_CHANGE_THRESHOLD[5:0] Function Description

CTS_CHANGE_THRESHOLD[5:0]	Description
100101 (default)	Tolerance of CTS value for CTS_PASS_THRSH_RAW and MT_MSK_NEW_CTS
xxxxxx	Tolerance of CTS value for CTS_PASS_THRSH_RAW and MT_MSK_NEW_CTS

CHANNEL STATUS

Channel status bits are extracted from the HDMI audio packets of the first audio channel (that is, Channel 0) and stored in the CHANNEL_STATUS_DATA_x registers of the HDMI map (where x = 1, 2, 3, 4, and 5).

Validity Status Flag

The channel status readback described in the Channel Status section must be considered valid if CS_DATA_VALID_RAW is set to 1. Figure 24 shows the algorithm that can be implemented to monitor the read valid channel status bit using the CS_DATA_VALID_RAW flag.

CS_DATA_VALID_RAW, IO, Address 0x65[7] (Read Only)

This bit is the raw status signal of the channel status data valid signal.

Table 151. CS_DATA_VALID_RAW Function Description

CS_DATA_VALID_RAW	Description
0 (default)	Channel status data is not valid.
1	Channel status data is valid.

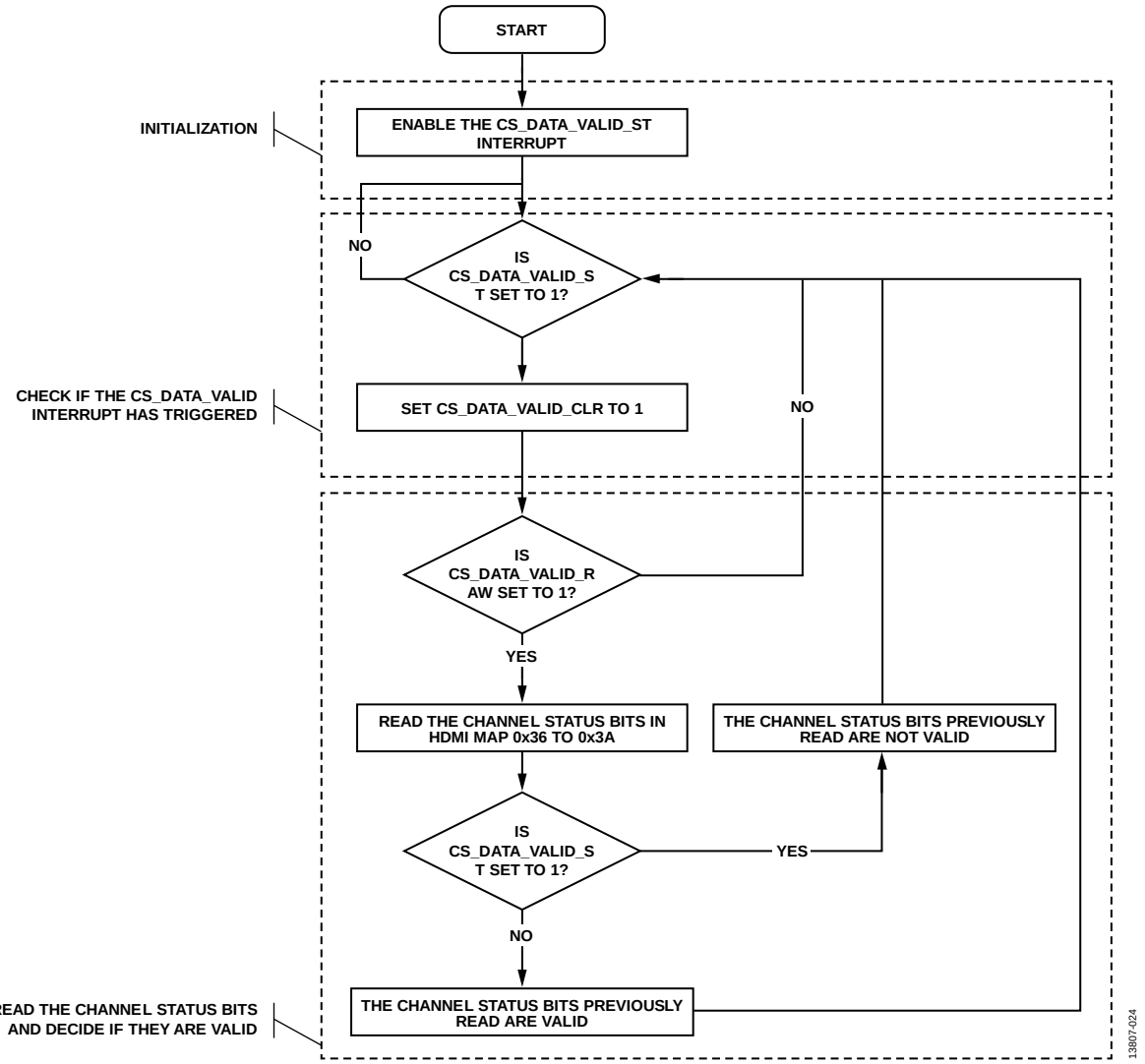


Figure 24. Reading Valid Channel Status Flags

Note that CS_DATA_VALID_RAW indicates that the first 40 of the channel status bits sent by the upstream transmitter have been correctly collected. This bit does not indicate if the content of the channel status bit is corrupted as this is indeterminable.

A corresponding interrupt can be enabled for CS_DATA_VALID_RAW by setting the mask CS_DATA_VALID_MB1 or CS_DATA_VALID_MB2. See the Interrupts section for additional information on the interrupt feature.

General Control and Mode Information

The general control and mode information are specified in Byte 0 of the channel status. For more information, see the IEC60958 standards.

CS_DATA[0], Consumer/Professional Application, HDMI Map, Address 0x36[0]

Table 152. CS_DATA[0] Function Description

CS_DATA[0]	Description
0 (default)	Consumer application
1	Professional application

CS_DATA[1], PCM/non-PCM Audio Sample, HDMI Map, Address 0x36[1]

Table 153. CS_DATA[1] Function Description

CS_DATA[1]	Description
0 (default)	Audio sample word represents linear PCM samples
1	Audio sample word used for other purposes

CS_DATA[2], Copyright, HDMI Map, Address 0x36[2]

Table 154. CS_DATA[2] Function Description

CS_DATA[2]	Description
0 (default)	Software for which copyright is asserted
1	Software for which no copyright is asserted

CS_DATA[5:3], Emphasis, HDMI Map, Address 0x36[5:3]

Table 155. CS_DATA[5:3] Function Description

CS_DATA[5:3][1]	Description
000 (default)	Two audio channels without pre-emphasis
001	Two audio channels with 50/15 pre-emphasis

[1] Unspecified values are reserved.

CS_DATA[7:6], Channel Status Mode, HDMI Map, Address 0x36[7:6]

Table 156. CS_DATA[7:6] Function Description

CS_DATA[7:6][1]	Description
00 (default)	Mode 0

[1] Unspecified values are reserved.

Category Code

The category code is specified in Byte 1 of the channel status. The category code indicates the type of equipment that generates the digital audio interface signal. For more information, refer to the IEC60958 standards.

CS_DATA[15:8], Category Code, HDMI Map, Address 0x37[7:0]

Table 157. CS_DATA[15:8] Function Description

CS_DATA[15:8]	Description
xxxx xxxx	Category code[1]
0000 0000 (default)	Reset value

[1] Refer to the IEC60958-3 standards.

Source Number and Channel Number

CS_DATA[19:16], Source Number, HDMI Map, Address 0x38[3:0]

Table 158. CS_DATA[19:16] Function Description

CS_DATA[19:16]	Description
xxxx	Source number[1]
0000 (default)	Reset value

[1] Refer to the IEC60958-3 standards.

CS_DATA[23:20], Channel Number, HDMI Map, Address 0x38[7:4]

Table 159. CS_DATA[23:20] Function Description

CS_DATA[23:20]	Description
xxxxx	Channel number[1]
00000 (default)	Reset value

[1] Refer to the IEC60958-3 standards.

Sampling and Frequency Accuracy

The sampling frequency and clock accuracy are specified by Byte 3 of the channel status. For additional information, refer to the IEC60958 standards.

CS_DATA[27:24], Sampling Frequency, HDMI Map, Address 0x39[3:0]

Table 160. CS_DATA[27:24] Function Description

CS_DATA[27:24][1]	Description
0000 (default)	44.1 kHz
0010	48 kHz
0011	32 kHz
1000	88.2 kHz
1001	768 kHz
1010	96 kHz
1100	176 kHz
1110	192 kHz

[1] Unspecified values are reserved.

CS_DATA[29:28], Clock Accuracy, HDMI Map, Address 0x39[5:4]

Table 161. CS_DATA[29:28] Function Description

CS_DATA[29:28]	Description
00 (default)	Level II, ±1000 ppm
01	Level I, ±50 ppm
10	Level III, variable pitch shifted
11	Reserved

CS_DATA[31:30], Reserved Register, HDMI Map, Address 0x39[7:6]

Table 162. CS_DATA[31:30] Function Description

CS_DATA[31:30]	Description
xx	Reserved
00 (default)	Reset value

Word Length

Word length information is specified in Byte 4 of the channel status bit. For more information, refer to the IEC60958 standards.

CS_DATA[32], Maximum Word Length Size, HDMI Map, Address 0x3A[0]

Table 163. CS_DATA[32] Function Description

CS_DATA[32]	Description
0 (default)	Maximum audio sample word length is 20 bits.
1	Maximum audio sample word length is 24 bits.

CS_DATA[35:33], Word Length, HDMI Map, Address 0x3A[3:1]

Table 164. CS_DATA[35:33] Function Description

	Description	
CS_DATA[35:33][1]	Audio Sample Word Length if Maximum Length is 24 as Indicated by CS_DATA_[32]	Audio Sample Word Length if Maximum Length is 20 as Indicated by CS_DATA_[32]
000 (default)	Word length not indicated	Word length not indicated
001	20 bits	16 bits
010	22 bits	18 bits
100	23 bits	19 bits
101	24 bits	20 bits
110	21 bits	21 bits

[1] Unspecified values are reserved.

Channel Status Copyright Value Assertion

It is possible to overwrite the copyright value of the channel status bit that is passed to the SPDIF output. This is done via the CS_COPYRIGHT_MANUAL and CS_COPYRIGHT_VALUE controls.

CS_COPYRIGHT_MANUAL, Address 68 (HDMI), Address 0x50[1]

This bit is a control to select automatic or manual setting of the copyright value of the channel status bit that is passed to the SPDIF output. Manual control is set with the CS_COPYRIGHT_VALUE bit.

Table 165. CS_COPYRIGHT_MANUAL Function Description

CS_COPYRIGHT_MANUAL	Description
0 (default)	Automatic CS copyright control.
1	Manual CS copyright control. Manual value is set by CS_COPYRIGHT_VALUE.

CS_COPYRIGHT_VALUE, Address 68 (HDMI), Address 0x50[0]

This bit is a control to set the CS copyright value when in manual configuration of the CS copyright bit that is passed to the SPDIF output.

Table 166. CS_COPYRIGHT_VALUE Function Description

CS_COPYRIGHT_VALUE	Description
0 (default)	Copyright value of channel status bit is 0. Valid only if CS_COPYRIGHT_MANUAL is set to 1.
1	Copyright value of channel status bit is 1. Valid only if CS_COPYRIGHT_MANUAL is set to 1.

Monitoring Change of Audio Sampling Frequency

The ADV7613 features the NEW_SAMP_RT_RAW flag to monitor changes in the audio sampling frequency field of the channel status bits.

NEW_SAMP_RT_RAW, IO, Address 0x83[3] (Read Only)

This bit is the status of the new sampling rate interrupt signal. When set to 1, it indicates that the audio sampling frequency field in channel status data has changed. Once set, this bit remains high until it is cleared via NEW_SAMP_RT_CLR.

Table 167. NEW_SAMP_RT_RAW Function Description

NEW_SAMP_RT_RAW	Description
0 (default)	Sampling rate bits of the channel status data on audio Channel 0 have not changed.
1	Sampling rate bits of the channel status data on audio Channel 0 have changed.

It is important to note that the NEW_SAMP_RT_RAW flag does not trigger if CS_DATA_VALID_RAW is set to 0. This prevents the notification of a change from a valid to an invalid audio sampling frequency readback in the channel status bits, and vice versa.

PACKETS AND INFOFRAMES REGISTERS

In HDMI, auxiliary data is carried across the digital link using a series of packets. The ADV7613 automatically detects and stores the following HDMI packets:

- InfoFrames
- Audio content protection (ACP)
- International standard recording code (ISRC)
- Gamut metadata

When the ADV7613 receives one of these packets, it computes the packet checksum and compares it with the checksum available in the packet. If these checksums are the same, the packets are stored in the corresponding registers. If the checksums are not the same, the packets are discarded. Refer to the EIA/CEA-861D specifications for more information on the packets fields.

InfoFrames Registers

The ADV7613 can store the following InfoFrames:

- Auxiliary video information (AVI) InfoFrame
- Source production descriptor (SPD) InfoFrame
- Audio InfoFrame
- Moving picture expert group (MPEG) source InfoFrame

InfoFrame Collection Mode

The ADV7613 has two modes for storing the InfoFrame packet sent from the source into the internal memory. By default, the ADV7613 only stores the InfoFrame packets received if the checksum is correct for each InfoFrame.

The ADV7613 also provides a mode to store every InfoFrame sent from the source, regardless of a InfoFrame packet checksum error.

ALWAYS_STORE_INF, Address 68 (HDMI), Address 0x47[0]

This bit is a control to force InfoFrames with checksum errors to be stored.

Table 168. ALWAYS_STORE_INF Function Description

ALWAYS_STORE_INF	Description
0 (default)	Stores data from received InfoFrames only if their checksum is correct
1	Always store the data from received InfoFrame regardless of their checksum

InfoFrame Checksum Error Flags

The following checksum error status registers flag when the last InfoFrame received has a checksum error. Once set, these bits remain high until the interrupt is cleared via their corresponding clear bits.

AVI_INF_CKS_ERR_RAW, IO, Address 0x88[4] (Read Only)

This bit is the status of the AVI InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for an AVI InfoFrame. Once set, this bit remains high until it is cleared via AVI_INF_CKS_ERR_CLR.

Table 169. AVI_INF_CKS_ERR_RAW Function Description

AVI_INF_CKS_ERR_RAW	Description
0 (default)	No AVI InfoFrame checksum error has occurred.
1	An AVI InfoFrame checksum error has occurred.

AUD_INF_CKS_ERR_RAW, IO, Address 0x88[5] (Read Only)

This bit is the status of the audio InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for an audio InfoFrame. Once set, this bit remains high until it is cleared via AUDIO_INF_CKS_ERR_CLR.

Table 170. AUD_INF_CKS_ERR_RAW Function Description

AUD_INF_CKS_ERR_RAW	Description
0 (default)	No audio InfoFrame checksum error has occurred.
1	An audio InfoFrame checksum error has occurred.

SPD_INF_CKS_ERR_RAW, IO, Address 0x88[6] (Read Only)

This bit is the status of SPD InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for an SPD InfoFrame. Once set, this bit remains high until it is cleared via ASPD_INF_CKS_ERR_CLR.

Table 171. SPD_INF_CKS_ERR_RAW Function Description

SPD_INF_CKS_ERR_RAW	Description
0 (default)	No SPD InfoFrame checksum error has occurred.
1	An SPD InfoFrame checksum error has occurred.

MS_INF_CKS_ERR_RAW, IO, Address 0x88[7] (Read Only)

This bit is the status of MPEG source InfoFrame checksum error interrupt signal. When set to 1. it indicates that a checksum error has been detected for an MPEG source InfoFrame. Once set, this bit remains high until it is cleared via MS_INF_CKS_ERR_CLR.

Table 172. MS_INF_CKS_ERR_RAW Function Description

MS_INF_CKS_ERR_RAW	Description
0 (default)	No MPEG source InfoFrame checksum error has occurred.
1	An MPEG source InfoFrame checksum error has occurred.

VS_INF_CKS_ERR_RAW, IO, Address 0x8D[0] (Read Only)

This bit is the status of vendor specific InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for an Vendor Specific InfoFrame. Once set, this bit remains high until it is cleared via VS_INF_CKS_ERR_CLR.

Table 173. VS_INF_CKS_ERR_RAW Function Description

VS_INF_CKS_ERR_RAW	Description
0 (default)	No VS InfoFrame checksum error has occurred
1	A VS InfoFrame checksum error has occurred

AVI InfoFrame Registers

Table 174 provides a list of readback registers for the AVI InfoFrame data. Refer to the EIA/CEA-861D specifications for a detailed explanation of the AVI InfoFrame fields.

Table 174. AVI InfoFrame Registers

InfoFrame Map Address	Access Type[1]	Register Name	Byte Name[2]
0xE0	R/W	AVI_PACKET_ID[7:0]	Packet type value
0xE1	R	AVI_INF_VER	InfoFrame version number
0xE2	R	AVI_INF_LEN	InfoFrame length
0x00	R	AVI_INF_PB_0_1	Checksum
0x01	R	AVI_INF_PB_0_2	Data Byte 1
0x02	R	AVI_INF_PB_0_3	Data Byte 2
0x03	R	AVI_INF_PB_0_4	Data Byte 3
0x04	R	AVI_INF_PB_0_5	Data Byte 4
0x05	R	AVI_INF_PB_0_6	Data Byte 5
0x06	R	AVI_INF_PB_0_7	Data Byte 6
0x07	R	AVI_INF_PB_0_8	Data Byte 7
0x08	R	AVI_INF_PB_0_9	Data Byte 8
0x09	R	AVI_INF_PB_0_10	Data Byte 9
0x0A	R	AVI_INF_PB_0_11	Data Byte 10
0x0B	R	AVI_INF_PB_0_12	Data Byte 11
0x0C	R	AVI_INF_PB_0_13	Data Byte 12
0x0D	R	AVI_INF_PB_0_14	Data Byte 13
0x0E	R	AVI_INF_PB_0_15	Data Byte 14
0x0F	R	AVI_INF_PB_0_16	Data Byte 15
0x10	R	AVI_INF_PB_0_17	Data Byte 16
0x11	R	AVI_INF_PB_0_18	Data Byte 17

InfoFrame Map Address	Access Type[1]	Register Name	Byte Name[2]
0x12	R	AVI_INF_PB_0_19	Data Byte 18
0x13	R	AVI_INF_PB_0_20	Data Byte 19
0x14	R	AVI_INF_PB_0_21	Data Byte 20
0x15	R	AVI_INF_PB_0_22	Data Byte 21
0x16	R	AVI_INF_PB_0_23	Data Byte 22
0x17	R	AVI_INF_PB_0_24	Data Byte 23
0x18	R	AVI_INF_PB_0_25	Data Byte 24
0x19	R	AVI_INF_PB_0_26	Data Byte 25
0x1A	R	AVI_INF_PB_0_27	Data Byte 26
0x1B	R	AVI_INF_PB_0_28	Data Byte 27

[1] R/W means memory location has read and write access. R means memory location is read access only; a read always returns 0, unless otherwise specified.
[2] As defined by the EIA/CEA-861D specifications.

The AVI InfoFrame registers are considered valid if the following two conditions are met: AVI_INFO_RAW is 1, and AVI_INF_CKS_ERR_RAW is 0 (this condition applies only if ALWAYS_STORE_INF is set to 1).

AVI_INFO_RAW is described in the Interrupt Architecture Overview section.

Audio InfoFrame Registers

Table 175 provides the list of readback registers available for the Audio InfoFrame. Refer to the EIA/CEA-861D specifications for a detailed explanation of the audio InfoFrame fields.

Table 175. Audio InfoFrame Registers

InfoFrame Map Address	Access Type[1]	Register Name	Byte Name[2]
0xE3	R/W	AUD_PACKET_ID[7:0]	Packet type value
0xE4	R	AUD_INF_VERS	InfoFrame version number
0xE5	R	AUD_INF_LEN	InfoFrame length
0x1C	R	AUD_INF_PB_0_1	Checksum
0x1D	R	AUD_INF_PB_0_2	Data Byte 1
0x1E	R	AUD_INF_PB_0_3	Data Byte 2
0x1F	R	AUD_INF_PB_0_4	Data Byte 3
0x20	R	AUD_INF_PB_0_5	Data Byte 4
0x21	R	AUD_INF_PB_0_6	Data Byte 5
0x22	R	AUD_INF_PB_0_7	Data Byte 6
0x23	R	AUD_INF_PB_0_8	Data Byte 7
0x24	R	AUD_INF_PB_0_9	Data Byte 8
0x25	R	AUD_INF_PB_0_10	Data Byte 9
0x26	R	AUD_INF_PB_0_11	Data Byte 10
0x27	R	AUD_INF_PB_0_12	Data Byte 11
0x28	R	AUD_INF_PB_0_13	Data Byte 12
0x29	R	AUD_INF_PB_0_14	Data Byte 13

[1] R/W means memory location has read and write access. R means memory location is read access only; a read always returns 0, unless otherwise specified.
[2] As defined by the EIA/CEA-861D specifications.

The audio InfoFrame registers are considered valid if the following two conditions are met: AUDIO_INFO_RAW is 1, and AUD_INF_CKS_ERR_RAW is 0 (this condition applies only if ALWAYS_STORE_INF is set to 1).

AUDIO_INFO_RAW, IO, Address 0x60[1] (Read Only)

This bit is the raw status of the audio InfoFrame detected signal.

Table 176. AUDIO_INFO_RAW Function Description

AUDIO_INFO_RAW	Description
0 (default)	No AVI InfoFrame were received within the last three VSYNCs or since the last HDMI packet detection reset.
1	An audio InfoFrame was received within the last three VSYNCs. This bit resets to zero on the fourth VSYNC leading edge following an audio InfoFrame, after an HDMI packet detection reset or upon writing to AUD_PACKET_ID.

SPD InfoFrame Registers

Table 177 provides a list of readback registers available for the SPD InfoFrame. Refer to the EIA/CEA-861D specifications for a detailed explanation of the SPD InfoFrame fields.

Table 177. SPD InfoFrame Registers

InfoFrame Map Address	Access Type[1]	Register Name	Byte Name[2]
0xE6	R/W	SPD_PACKET_ID[7:0]	Packet type value
0xE7	R	SPD_INF_VER	InfoFrame version number
0xE8	R	SPD_INF_LEN	InfoFrame length
0x2A	R	SPD_INF_PB_0_1	Checksum
0x2B	R	SPD_INF_PB_0_2	Data Byte 1
0x2C	R	SPD_INF_PB_0_3	Data Byte 2
0x2D	R	SPD_INF_PB_0_4	Data Byte 3
0x2E	R	SPD_INF_PB_0_5	Data Byte 4
0x2F	R	SPD_INF_PB_0_6	Data Byte 5
0x30	R	SPD_INF_PB_0_7	Data Byte 6
0x31	R	SPD_INF_PB_0_8	Data Byte 7
0x32	R	SPD_INF_PB_0_9	Data Byte 8
0x33	R	SPD_INF_PB_0_10	Data Byte 9
0x34	R	SPD_INF_PB_0_11	Data Byte 10
0x35	R	SPD_INF_PB_0_12	Data Byte 11
0x36	R	SPD_INF_PB_0_13	Data Byte 12
0x37	R	SPD_INF_PB_0_14	Data Byte 13
0x38	R	SPD_INF_PB_0_15	Data Byte 14
0x39	R	SPD_INF_PB_0_16	Data Byte 15
0x3A	R	SPD_INF_PB_0_17	Data Byte 16
0x3B	R	SPD_INF_PB_0_18	Data Byte 17
0x3C	R	SPD_INF_PB_0_19	Data Byte 18
0x3D	R	SPD_INF_PB_0_20	Data Byte 19
0x3E	R	SPD_INF_PB_0_21	Data Byte 20
0x3F	R	SPD_INF_PB_0_22	Data Byte 21
0x40	R	SPD_INF_PB_0_23	Data Byte 22
0x41	R	SPD_INF_PB_0_24	Data Byte 23
0x42	R	SPD_INF_PB_0_25	Data Byte 24
0x43	R	SPD_INF_PB_0_26	Data Byte 25
0x44	R	SPD_INF_PB_0_27	Data Byte 26
0x45	R	SPD_INF_PB_0_28	Data Byte 27

[1] R/W means memory location has read and write access. R means memory location is read access only; a read always returns 0, unless otherwise specified.
[2] As defined by the EIA/CEA-861D specifications.

The source product descriptor InfoFrame registers are considered valid if the following two conditions are met: SPD_INFO_RAW is 1, and SPD_INF_CKS_ERR_RAW is 0 (this condition only applies if ALWAYS_STORE_INF is set to 1).

SPD_INFO_RAW, IO, Address 0x60[2] (Read Only)

This bit is the raw status of the SPD InfoFrame detected signal.

Table 178. SPD_INFO_RAW Function Description

SPD_INFO_RAW	Description
0 (default)	No source product description InfoFrame received since the last HDMI packet detection reset.
1	Source product description InfoFrame received. This bit resets to zero after an HDMI packet detection reset or upon writing to SPD_PACKET_ID.

MPEG Source InfoFrame Registers

Table 179 provides a list of readback registers available for the MPEG InfoFrame. Refer to the EIA/CEA-861D specifications for a detailed explanation of the MPEG InfoFrame fields.

Table 179. MPEG InfoFrame Registers

InfoFrame Map Address	Access Type[1]	Register Name	Byte Name[2]
0xE9	R/W	MS_PACKET_ID[7:0]	Packet type value
0xEA	R	MS_INF_VERS	InfoFrame version number
0xEB	R	MS_INF_LEN	InfoFrame length
0x46	R	MS_INF_PB_0_1	Checksum
0x47	R	MS_INF_PB_0_2	Data Byte 1
0x48	R	MS_INF_PB_0_3	Data Byte 2
0x49	R	MS_INF_PB_0_4	Data Byte 3
0x4A	R	MS_INF_PB_0_5	Data Byte 4
0x4B	R	MS_INF_PB_0_6	Data Byte 5
0x4C	R	MS_INF_PB_0_7	Data Byte 6
0x4D	R	MS_INF_PB_0_8	Data Byte 7
0x4E	R	MS_INF_PB_0_9	Data Byte 8
0x4F	R	MS_INF_PB_0_10	Data Byte 9
0x50	R	MS_INF_PB_0_11	Data Byte 10
0x51	R	MS_INF_PB_0_12	Data Byte 11
0x52	R	MS_INF_PB_0_13	Data Byte 12
0x53	R	MS_INF_PB_0_14	Data Byte 13

[1] R/W means memory location has read and write access. R means memory location is read access only; a read always returns 0, unless otherwise specified.
[2] As defined by the EIA/CEA-861D specifications.

The MPEG InfoFrame registers are considered valid if the following two conditions are met: MS_INFO_RAW is 1, and MS_INF_CKS_ERR_RAW is 0 (this condition applies only if ALWAYS_STORE_INF is set to 1).

MS_INFO_RAW, IO, Address 0x60[3] (Read Only)

This bit is the raw status signal of the MPEG source InfoFrame detection signal.

Table 180. MS_INFO_RAW Function Description

MS_INFO_RAW	Description
0 (default)	No source product description InfoFrame received within the last three VSYNCs or since the last HDMI packet detection reset.
1	MPEG Source InfoFrame received. This bit resets to zero after an HDMI packet detection reset or upon writing to MS_PACKET_ID.

Vendor Specific InfoFrame Registers

Table 181 provides a list of readback registers available for the vendor specific InfoFrame.

Table 181. VS InfoFrame Registers

InfoFrame Map Address	Access Type[1]	Register Name	Byte Name
0xEC	R	VS_PACKET_ID[7:0]	Packet type value
0xED	R	VS_INF_VERS	InfoFrame version number
0xEE	R	VS_INF_LEN	InfoFrame length
0x54	R	VS_INF_PB_0_1	Checksum
0x55	R	VS_INF_PB_0_2	Data Byte 1
0x56	R	VS_INF_PB_0_3	Data Byte 2
0x57	R	VS_INF_PB_0_4	Data Byte 3
0x58	R	VS_INF_PB_0_5	Data Byte 4
0x59	R	VS_INF_PB_0_6	Data Byte 5
0x5A	R	VS_INF_PB_0_7	Data Byte 6
0x5B	R	VS_INF_PB_0_8	Data Byte 7
0x5C	R	VS_INF_PB_0_9	Data Byte 8
0x5D	R	VS_INF_PB_0_10	Data Byte 9
0x5E	R	VS_INF_PB_0_11	Data Byte 10
0x5F	R	VS_INF_PB_0_12	Data Byte 11
0x60	R	VS_INF_PB_0_13	Data Byte 12
0x61	R	VS_INF_PB_0_14	Data Byte 13
0x62	R	VS_INF_PB_0_15	Data Byte 14
0x63	R	VS_INF_PB_0_16	Data Byte 15
0x64	R	VS_INF_PB_0_17	Data Byte 16
0x65	R	VS_INF_PB_0_18	Data Byte 17
0x66	R	VS_INF_PB_0_19	Data Byte 18
0x67	R	VS_INF_PB_0_20	Data Byte 19
0x68	R	VS_INF_PB_0_21	Data Byte 20
0x69	R	VS_INF_PB_0_22	Data Byte 21
0x6A	R	VS_INF_PB_0_23	Data Byte 22
0x6B	R	VS_INF_PB_0_24	Data Byte 23
0x6C	R	VS_INF_PB_0_25	Data Byte 24
0x6D	R	VS_INF_PB_0_26	Data Byte 25
0x6E	R	VS_INF_PB_0_27	Data Byte 26
0x6F	R	VS_INF_PB_0_28	Data Byte 27

[1] R means memory location is read access only; a read always returns 0, unless otherwise specified.

The vendor specific InfoFrame registers are considered valid if the following two conditions are met: VS_INFO_RAW is 1, and VS_INF_CKS_ERR_RAW is 0 (this condition applies only if ALWAYS_STORE_INF is set to 1).

VS_INFO_RAW, IO, Address 0x60[4] (Read Only)

This bit is the raw status signal of the vendor specific InfoFrame detection signal.

Table 182. VS_INFO_RAW Function Description

VS_INFO_RAW	Description
0 (default)	No new VS InfoFrame has been received since the last HDMI packet detection reset.
1	A new VS InfoFrame has been received. This bit resets to zero after an HDMI packet detection reset or upon writing to VS_PACKET_ID.

PACKET REGISTERS

ACP Packet Registers

Table 183 provides the list of readback registers available for the ACP packets. Refer to the HDMI 1.3 specifications for a detailed explanation of the ACP packet fields.

Table 183. ACP Packet Registers

InfoFrame Map Address	Access Type[1]	Register Name	Packet Byte No.[2]
0xEF	R/W	ACP_PACKET_ID[7:0]	Packet type value
0xF0	R	ACP_TYPE	HB1
0xF1	R	ACP_HEADER2	HB2
0x70	R	ACP_PB_0_1	PB0
0x71	R	ACP_PB_0_2	PB1
0x72	R	ACP_PB_0_3	PB2
0x73	R	ACP_PB_0_4	PB3
0x74	R	ACP_PB_0_5	PB4
0x75	R	ACP_PB_0_6	PB5
0x76	R	ACP_PB_0_7	PB6
0x77	R	ACP_PB_0_8	PB7
0x78	R	ACP_PB_0_9	PB8
0x79	R	ACP_PB_0_10	PB9
0x7A	R	ACP_PB_0_11	PB10
0x7B	R	ACP_PB_0_12	PB11
0x7C	R	ACP_PB_0_13	PB12
0x7D	R	ACP_PB_0_14	PB13
0x7E	R	ACP_PB_0_15	PB14
0x7F	R	ACP_PB_0_16	PB15
0x80	R	ACP_PB_0_17	PB16
0x81	R	ACP_PB_0_18	PB17
0x82	R	ACP_PB_0_19	PB18
0x83	R	ACP_PB_0_20	PB19
0x84	R	ACP_PB_0_21	PB20
0x85	R	ACP_PB_0_22	PB21
0x86	R	ACP_PB_0_23	PB22
0x87	R	ACP_PB_0_24	PB23
0x88	R	ACP_PB_0_25	PB24
0x89	R	ACP_PB_0_26	PB25
0x8A	R	ACP_PB_0_27	PB26
0x8B	R	ACP_PB_0_28	PB27

[1] R/W means memory location has read and write access. R means memory location is read access only; a read always returns 0, unless otherwise specified.
[2] As defined by the HDMI 1.3 specifications.

The ACP InfoFrame registers are considered valid if ACP_PCKT_RAW is set to 1.

ACP_PCKT_RAW, IO, Address 0x60[5] (Read Only)

This bit is the raw status signal of the audio content protection packet detection signal.

Table 184. ACP_PCKT_RAW Function Description

ACP_PCKT_RAW	Description
0 (default)	No ACP packet received within the last 600 ms or since the last HDMI packet detection reset.
1	ACP packets have been received within the last 600 ms. This bit resets to zero after an HDMI packet detection reset or upon writing to ACP_PACKET_ID.

ISRC Packet Registers

Table 185 and Table 187 provide lists of readback registers available for the ISRC packets. Refer to the HDMI 1.3 specifications for a detailed explanation of the ISRC packet fields.

Table 185. ISRC1 Packet Registers

InfoFrame Map Address	Access Type[1]	Register Name	Packet Byte No.[2]
0xF2	R/W	ISRC1_PACKET_ID[7:0]	Packet type value
0xF3	R	ISRC1_HEADER1	HB1
0xF4	R	ISRC1_HEADER2	HB2
0x8C	R	ISRC1_PB_0_1	PB0
0x8D	R	ISRC1_PB_0_2	PB1
0x8E	R	ISRC1_PB_0_3	PB2
0x8F	R	ISRC1_PB_0_4	PB3
0x90	R	ISRC1_PB_0_5	PB4
0x91	R	ISRC1_PB_0_6	PB5
0x92	R	ISRC1_PB_0_7	PB6
0x93	R	ISRC1_PB_0_8	PB7
0x94	R	ISRC1_PB_0_9	PB8
0x95	R	ISRC1_PB_0_10	PB9
0x96	R	ISRC1_PB_0_11	PB10
0x97	R	ISRC1_PB_0_12	PB11
0x98	R	ISRC1_PB_0_13	PB12
0x99	R	ISRC1_PB_0_14	PB13
0x9A	R	ISRC1_PB_0_15	PB14
0x9B	R	ISRC1_PB_0_16	PB15
0x9C	R	ISRC1_PB_0_17	PB16
0x9D	R	ISRC1_PB_0_18	PB17
0x9E	R	ISRC1_PB_0_19	PB18
0x9F	R	ISRC1_PB_0_20	PB19
0xA0	R	ISRC1_PB_0_21	PB20
0xA1	R	ISRC1_PB_0_22	PB21
0xA2	R	ISRC1_PB_0_23	PB22
0xA3	R	ISRC1_PB_0_24	PB23
0xA4	R	ISRC1_PB_0_25	PB24
0xA5	R	ISRC1_PB_0_26	PB25
0xA6	R	ISRC1_PB_0_27	PB26
0xA7	R	ISRC1_PB_0_28	PB27

[1] R/W means memory location has read and write access. R means memory location is read access only; a read always returns 0, unless otherwise specified.
[2] As defined by the HDMI specifications.

The ISRC1 packet registers are considered valid if ISRC1_PCKT_RAW is set to 1.

ISRC1_PCKT_RAW, IO, Address 0x60[6] (Read Only)

This bit is the raw status signal of International Standard Recording Code 1 (ISRC1) packet detection signal.

Table 186. ISRC1_PCKT_RAW Function Description

ISRC1_PCKT_RAW	Description
0 (default)	No ISRC1 packets received since the last HDMI packet detection reset.
1	ISRC1 packets have been received. This bit resets to zero after an HDMI packet detection reset or upon writing to ISRC1_PACKET_ID.

Table 187. ISRC2 Packet Registers

InfoFrame Map Address	Access Type[1]	Register Name	Packet Byte No.[2]
0xF5	R/W	ISRC2_PACKET_ID[7:0]	Packet type value
0xF6	R	ISRC2_HEADER1	HB1
0xF7	R	ISRC2_HEADER2	HB2
0xA8	R	ISRC2_PB_0_1	PB0
0xA9	R	ISRC2_PB_0_2	PB1
0xAA	R	ISRC2_PB_0_3	PB2
0xAB	R	ISRC2_PB_0_4	PB3
0xAC	R	ISRC2_PB_0_5	PB4
0xAD	R	ISRC2_PB_0_6	PB5
0xAE	R	ISRC2_PB_0_7	PB6
0xAF	R	ISRC2_PB_0_8	PB7
0xB0	R	ISRC2_PB_0_9	PB8
0xB1	R	ISRC2_PB_0_10	PB9
0xB2	R	ISRC2_PB_0_11	PB10
0xB3	R	ISRC2_PB_0_12	PB11
0xB4	R	ISRC2_PB_0_13	PB12
0xB5	R	ISRC2_PB_0_14	PB13
0xB6	R	ISRC2_PB_0_15	PB14
0xB7	R	ISRC2_PB_0_16	PB15
0xB8	R	ISRC2_PB_0_17	PB16
0xB9	R	ISRC2_PB_0_18	PB17
0xBA	R	ISRC2_PB_0_19	PB18
0xBB	R	ISRC2_PB_0_20	PB19
0xBC	R	ISRC2_PB_0_21	PB20
0xBD	R	ISRC2_PB_0_22	PB21
0xBE	R	ISRC2_PB_0_23	PB22
0xBF	R	ISRC2_PB_0_24	PB23
0xC0	R	ISRC2_PB_0_25	PB24
0xC1	R	ISRC2_PB_0_26	PB25
0xC2	R	ISRC2_PB_0_27	PB26
0xC3	R	ISRC2_PB_0_28	PB27

[1] R/W means memory location has read and write access. R means memory location is read access only; a read always returns 0, unless otherwise specified.
[2] As defined by the HDMI 1.3 specifications.

The ISRC2 packet registers are considered valid if, and only, if ISRC1_PCKT_RAW is set to 1.

ISRC2_PCKT_RAW, IO, Address 0x60[7] (Read Only)

This bit is the raw status signal of International Standard Recording Code 2 (ISRC2) packet detection signal.

Table 188. ISRC2_PCKT_RAW Function Description

ISRC2_PCKT_RAW	Description
0 (default)	No ISRC2 packets received since the last HDMI packet detection reset.
1	ISRC2 packets have been received. This bit resets to zero after an HDMI packet detection reset or upon writing to ISRC2_PACKET_ID.

Gamut Metadata Packets

Refer to the HDMI specifications for a detailed explanation of the gamut metadata packet fields.

Table 189. Gamut Metadata Packet Registers

HDMI Map Address	Access Type[1]	Register Name	Packet Byte No.[2]
0xF8	R/W	GAMUT_PACKET_ID[7:0]	Packet type value
0xF9	R	GAMUT_HEADER1	HB1
0xFA	R	GAMUT_HEADER2	HB2
0xC4	R	GAMUT_MDATA_PB_0_1	PB0
0xC5	R	GAMUT_MDATA_PB_0_2	PB1
0xC6	R	GAMUT_MDATA_PB_0_3	PB2
0xC7	R	GAMUT_MDATA_PB_0_4	PB3
0xC8	R	GAMUT_MDATA_PB_0_5	PB4
0xC9	R	GAMUT_MDATA_PB_0_6	PB5
0xCA	R	GAMUT_MDATA_PB_0_7	PB6
0xCB	R	GAMUT_MDATA_PB_0_8	PB7
0xCC	R	GAMUT_MDATA_PB_0_9	PB8
0xCD	R	GAMUT_MDATA_PB_0_10	PB9
0xCE	R	GAMUT_MDATA_PB_0_11	PB10
0xCF	R	GAMUT_MDATA_PB_0_12	PB11
0xD0	R	GAMUT_MDATA_PB_0_13	PB12
0xD1	R	GAMUT_MDATA_PB_0_14	PB13
0xD2	R	GAMUT_MDATA_PB_0_15	PB14
0xD3	R	GAMUT_MDATA_PB_0_16	PB15
0xD4	R	GAMUT_MDATA_PB_0_17	PB16
0xD5	R	GAMUT_MDATA_PB_0_18	PB17
0xD6	R	GAMUT_MDATA_PB_0_19	PB18
0xD7	R	GAMUT_MDATA_PB_0_20	PB19
0xD8	R	GAMUT_MDATA_PB_0_21	PB20
0xD9	R	GAMUT_MDATA_PB_0_22	PB21
0xDA	R	GAMUT_MDATA_PB_0_23	PB22
0xDB	R	GAMUT_MDATA_PB_0_24	PB23
0xDC	R	GAMUT_MDATA_PB_0_25	PB24
0xDD	R	GAMUT_MDATA_PB_0_26	PB25
0xDE	R	GAMUT_MDATA_PB_0_27	PB26
0xDF	R	GAMUT_MDATA_PB_0_28	PB27

[1] R/W means memory location has read and write access. R means memory location is read access only; a read always returns 0, unless otherwise specified.
[2] As defined by the HDMI specifications.

The gamut metadata packet registers are considered valid if GAMUT_MDATA_RAW is set to 1.

GAMUT_MDATA_RAW, IO, Address 0x65[0] (Read Only)

This bit is the raw status signal of gamut metadata packet detection signal.

Table 190. GAMUT_MDATA_RAW Function Description

GAMUT_MDATA_RAW	Description
0 (default)	No gamut metadata packet has been received in the last video frame or since the last HDMI packet detection reset.
1	A gamut metadata packet has been received in the last video frame. This bit resets to zero after an HDMI packet detection reset or upon writing to GAMUT_PACKET_ID.

GAMUT_IRQ_NEXT_FIELD, Address 68 (HDMI), Address 0x50[4]

This bit is a control to set the NEW_GAMUT_MDATA_RAW interrupt to detect when the new contents are applicable to next field or to indicate that the gamut packet is new, by using the header information of the gamut packet.

Table 191. GAMUT_IRQ_NEXT_FIELD Function Description

GAMUT_IRQ_NEXT_FIELD	Description
0 (default)	Interrupt flag indicates that gamut packet is new.
1	Interrupt flag indicates that gamut packet is to be applied next field.

CUSTOMIZING PACKET/INFOFRAME STORAGE REGISTERS

The packet type value of each set of packet and InfoFrame registers in the InfoFrame map is programmable. This allows the user to configure the ADV7613 to store the payload data of any packet and InfoFrames sent by the transmitter connected on the selected HDMI port.

Note that writing to any of the nine following packet ID registers also clears the corresponding raw InfoFrame/packet detection bit. For example, writing 0x82, or any other value, to AVI_PACKET_ID clears AVI_INFO_RAW.

AVI_PACKET_ID[7:0], Address 7C (InfoFrame), Address 0xE0[7:0]

AVI_PACKET_ID[7:0] is the AVI InfoFrame ID.

Table 192. AVI_PACKET_ID[7:0] Function Description

AVI_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x00 to Address 0x1B
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x00 to Address 0x1B

AUD_PACKET_ID[7:0], Address 7C (InfoFrame), Address 0xE3[7:0]

AUD_PACKET_ID[7:0] is the audio InfoFrame ID.

Table 193. AUD_PACKET_ID[7:0] Function Description

AUD_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x1C to Address 0x29
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x1C to Address 0x29

SPD_PACKET_ID[7:0], Address 7C (InfoFrame), Address 0xE6[7:0]

SPD_PACKET_ID[7:0] is the source prod InfoFrame ID.

Table 194. SPD_PACKET_ID[7:0] Function Description

SPD_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x2A to Address 0x45
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x2A to Address 0x45

MS_PACKET_ID[7:0], Address 7C (InfoFrame), Address 0xE9[7:0]

MS_PACKET_ID[7:0] is the MPEG source InfoFrame ID.

Table 195. MS_PACKET_ID[7:0] Function Description

MS_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x46 to Address 0x53
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x46 to Address 0x53

VS_PACKET_ID[7:0], Address 7C (InfoFrame), Address 0xEC[7:0]

VS_PACKET_ID[7:0] is the vendor specific InfoFrame ID.

Table 196. VS_PACKET_ID[7:0] Function Description

VS_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x54 to Address 0x6F
1xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x54 to Address 0x6F

ACP_PACKET_ID[7:0], Address 7C (InfoFrame), Address 0xEF[7:0]

ACP_PACKET_ID[7:0] is the ACP InfoFrame ID.

Table 197. ACP_PACKET_ID[7:0] Function Description

ACP_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x70 to Address 0x8B
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x70 to Address 0x8B

ISRC1_PACKET_ID[7:0], Address 7C (InfoFrame), Address 0xF2[7:0]

ISRC1_PACKET_ID[7:0] is the ISRC1 InfoFrame ID.

Table 198. ISRC1_PACKET_ID[7:0] Function Description

ISRC1_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x8C to Address 0xA7
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x8C to Address 0xA7

ISRC2_PACKET_ID[7:0], Address 7C (InfoFrame), Address 0xF5[7:0]

ISRC2_PACKET_ID[7:0] is the ISRC2 InfoFrame ID.

Table 199. ISRC2_PACKET_ID[7:0] Function Description

ISRC2_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0xA8 to Address 0xC3
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0xA8 to Address 0xC3

GAMUT_PACKET_ID[7:0], Address 7C (InfoFrame), Address 0xF8[7:0]

GAMUT_PACKET_ID[7:0] is the Gamut InfoFrame ID.

Table 200. GAMUT_PACKET_ID[7:0] Function Description

GAMUT_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0xC4 to Address 0xDF
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0xC4 to Address 0xDF

Note that the packet type values and corresponding packets must not be programmed in the packet type values registers. These packets are always processed internally and cannot be stored in the packet/InfoFrame registers in the InfoFrame map.

- 0x01: audio clock regeneration packet
- 0x02: audio sample packet
- 0x03: general control packet
- 0x07: DSD audio sample packet
- 0x08: DST audio packet
- 0x09: HBR audio stream packet

REPEATER SUPPORT

The ADV7613 incorporates an EDID/repeater controller that provides all the features required for a receiver front end of a fully HDCP 1.4-compliant repeater system. The ADV7613 has a RAM that can store up to 127 KSVs, which allows it to handle up to 127 downstream devices in repeater mode (see Table 210).

The ADV7613 features a set of HDCP registers, defined in the HDCP specifications, which are accessible through the DDC bus (see the DDC Ports section) of the selected port. A subset of the HDCP registers (defined in the following subsections) are also available in the Repeater map and are accessible through the main I^2C port (see the Main I^2C Port section).

Repeater Routines Performed by the EDID/Repeater Controller

Power Up

A power-on reset circuitry on the DVDD supply is used to reset the EDID/repeater controller when the ADV7613 is powered up. When the EDID/repeater controller reboots after reset, it resets all the KSV registers listed in Table 210 to 0x00.

AKSV Update

The EDID/repeater controller resets automatically the BCAPS [5] bit to 0 when an HDCP transmitter writes its AKSV into the ADV7613 HDCP registers through the DDC bus of the HDMI port.

Note that writing a value in the AKSV[39:32] triggers an AKSV update and AKSV_UPDATE_ST interrupt if AKSV_UPDATE_MB1 or AKSV_UPDATE_MB2 has been set to 1 This triggers the EDID/repeater controller to reset the BCAPS [5] bit back to 0.

KSV List Ready

The KSV_LIST_READY bit is set by an external controller driving the ADV7613. This notifies the ADV7613 on-chip EDID/repeater controller that the KSV list registers have been updated with the KSV's of the attached and active downstream HDCP devices.

When KSV_LIST_READY is set to 1, the EDID/repeater controller computes the SHA-1 (refer to the HDCP documentation) hash value V', updates the corresponding V' registers (see Table 211), and sets the READY bit (that is, BCAPS[5]) to 1. This indicates to the transmitter attached to the ADV7613 that the KSV FIFO and SHA-1 hash value V' are ready to be read.

KSV_LIST_READY, Address 64 (Repeater), Address 0x71[7]

The system sets this bit to indicate that the KSV list has been read from the Tx IC(s) and written into the repeater map. The system must also set Bits[11:0] of BSTATUS before setting this bit.

Table 201. KSV_LIST_READY Function Description

KSV_LIST_READY	Description
0 (default)	Not ready
1	Ready

Note that the SHA-1 hash value is computed if the bit KSV_LIST_READY is set after the device receives an AKSV update from the upstream source. The external controller must therefore set KSV_LST_READY to 1 only after the device has received an AKSV update from the upstream source.

The ADV7613 does not automatically clear KSV_LIST_READY to 0, after it has finished computing the SHA-1 value. Therefore, the external controller needs to clear KSV_LIST_READY.

HDMI Mode

The BSTATUS[12]bit is updated automatically by the ADV7613 and follows the HDMI mode status of the HDMI/DVI stream input on the active HDMI port. BSTATUS [12] is set to 1 if the ADV7613 receives an HDMI stream, and set to 0 if the ADV7613 receives a DVI stream.

Repeater Actions Required by External Controller

The external controller must set the BCAPS register and notify the ADV7613 when the KSV list is updated, as described in the following sections: the Repeater Bit section, the KSV FIFO Read from HDCP Registers section, and the First AKSV Update section.

Note that many more routines must be implemented into the external controller driving the ADV7613 to implement a full repeater. Such routines are described in the HDCP and HDMI specifications (for example, copying InfoFrame and packet data image from the HDMI receiver into the HDMI transmitter, momentarily deasserting the hot plug detect and disabling the clock termination on a change of downstream topology, and so on).

Repeater Bit

The repeater bit (that is, BCAPS[6]) must be set to 1 by the external controller in the routine that initializes the ADV7613. The repeater bit must be left as such as long as the ADV7613 is configured as the front end of a repeater system.

Note that the registers in the KSV list (see Table 210) must always be set to 0x0 if the repeater bit is set to 0. The firmware running on the external controller, therefore, always sets the registers in the KSV list to 0x0 if the repeater bit is changed from 1 to 0.

KSV FIFO Read from HDCP Registers

The KSV FIFO read at Address 0x43 through the HDCP port of the selected HDMI port is dependent on the value of the repeater bit (that is, BCAPS[6]). When the repeater bit is set to 0, the KSV FIFO read from the HDCP port always returns 0x0. When the repeater bit is set to 1, the KSV FIFO read from the HDCP port matches the KSV list which is set in the Repeater map at Address 0x80 to Address 0xF7 (see Table 210).

First AKSV Update

When the upstream transmitter writes its AKSV for the first time into the ADV7613 HDCP registers, the external controller driving the ADV7613 must perform the following tasks:

- Update BSTATUS[11:0] according to the topology of the downstream device attached to the repeater.
- Update the KSV list (refer to Table 210) with the KSV from the transmitter on the back end of the repeater as well as the KSV from all the downstream devices connected to the repeater.
- Set KSV_LIST_READY to 1.
- The external controller can monitor the AKSV_UPDATE_A_RAW bits to be notified when the transmitter writes its AKSV into the HDCP registers of the ADV7613.

AKSV_UPDATE_A_RAW, IO, Address 0x88[0] (Read Only)

This bit is the status of the Port A AKSV update interrupt signal. When set to 1, it indicates that thetransmitter has written its AKSV into the HDCP registers for Port A. Once set, this bit remains high until it is cleared via AKSV_UPDATE_A_CLR.

Table 202. AKSV_UPDATE_A_RAW Function Description

AKSV_UPDATE_A_RAW	Description
0 (default)	No AKSV updates on Port A
1	Detected a write access to the AKSV register on Port A

Second and Subsequent AKSV Updates

When the upstream transmitter writes its AKSV for the second time or more into the ADV7613 HDCP registers, the external controller driving the ADV7613 must set KSV_LIST_READY to 1.

HDCP Registers Available in Repeater Map

To enable fast switching of the HDCP encrypted HDMI ports, Register 0x00 to Register 0x42 in the repeater map are replicated for each port. AUTO_HDCP_MAP_ENABLE and HDCP_MAP_SELECT determine which port is currently visible to the user.

AUTO_HDCP_MAP_ENABLE, Address 64 (Repeater), Address 0x79[3]

This bit selects which port is accessed for HDCP addresses: the HDMI active port (selected by HDMI_PORT_SELECT, HDMI map) or the one selected in HDCP_MAP_SELECT.

Table 203. AUTO_HDCP_MAP_ENABLE Function Description

AUTO_HDCP_MAP_ENABLE	Description
0	HDCP data read from port given by HDCP_MAP_SELECT
1 (default)	HDCP data read from the active HDMI port

HDCP_MAP_SELECT, Address 64 (Repeater), Address 0x79[0]

This bit selects which port is accessed for HDCP addresses (0x00 to 0x42 in repeater map). This only takes effect when AUTO_HDCP_MAP_ENABLE is 0.

Table 204. HDCP_MAP_SELECT Function Description

HDCP_MAP_SELECT[0]	Description
000 (default)	Select Port A

BKSV[39:0], Address 64 (Repeater), Address 0x04[7:0]; Address 0x03[7:0]; Address 0x02[7:0]; Address 0x01[7:0]; Address 0x00[7:0] (Read Only)

The receiver key selection vector (BKSV) can be read back once the device has accessed the HDCP ROM. The following registers contain the BKSV read from the EEPROM.

Table 205. BKSV[39:0] Function Description

BKSV[39:0]	Description
0x00[7:0]	BKSV[7:0]
0x01[7:0]	BKSV[15:8]
0x02[7:0]	BKSV[23:16]
0x03[7:0]	BKSV[31:24]
0x04[7:0]	BKSV[39:32]

AKSV[39:0], Address 64 (Repeater), Address 0x14[7:0]; Address 0x13[7:0]; Address 0x12[7:0]; Address 0x11[7:0]; Address 0x10[7:0]

The AKSV of the transmitter attached to the active HDMI port can be read back after an AKSV update. The following registers contain the AKSV written by the Tx.

Table 206. AKSV[39:0] Function Description

AKSV[39:0]	Description
0x10[7:0]	AKSV[7:0]
0x11[7:0]	AKSV[15:8]
0x12[7:0]	AKSV[23:16]
0x13[7:0]	AKSV[31:24]
0x14[7:0]	AKSV[39:32]

BCAPS[7:0], Address 64 (Repeater), Address 0x40[7:0]

This is the BCAPS register presented to the Tx attached to the active HDMI port.

Table 207. BCAPS[7:0] Function Description

BCAPS[7:0]	Description
10000011 (default)	Default BCAPS register value presented to the Tx
xxxxxxxx	BCAPS register value presented to the Tx

BSTATUS[15:0], Address 64 (Repeater), Address 0x42[7:0]; Address 0x41[7:0]

These registers contain the BSTATUS information presented to the Tx attached to the active HDMI port. Bits [11:0] must be set by the system software acting as a repeater.

Table 208. BSTATUS[15:0] Function Description

BSTATUS[15:0]	Description
xxxxxxxxxxxxxxxx	BSTATUS register presented to Tx.
0000000000000000 (default)	Reset value. BSTATUS register is reset only after power up.
0x41[7:0]	BSTATUS[7:0].
0x42[7:0]	BSTATUS[15:8].

The KSV registers are stored consecutively in RAM, which is split into 5x128 bytes bank maps. The maps are accessible through KSV_BYTE_0 to KSV_BYTE_127. The proper segment can be selected via the KSV_MAP_SELECT[2:0] register, as shown in Figure 25.

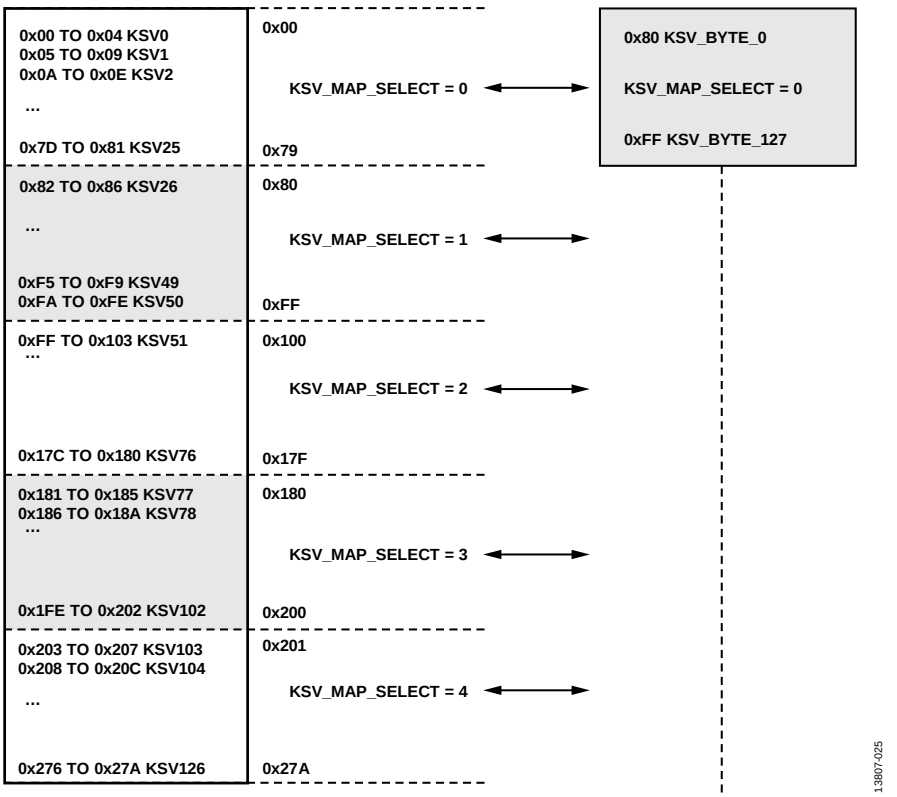


Figure 25. Addressing Block Using KSV_MAP_SELECT and Register KSV_BYTE_0 to Register KSV_BYTE_127

KSV_MAP_SELECT[2:0], Address 64 (Repeater), Address 0x79[6:4]

KSV_MAP_SELECT[2:0] selects which 128 bytes of KSV list are accessed when reading or writing to Address 0x80 to Address 0xFF in this map. Values from 5 and upwards are not valid.

Table 209. KSV_MAP_SELECT[2:0] Function Description

KSV_MAP_SELECT[2:0]	Description
000 (default)	KSV Map 0 selected
001	KSV Map 1 selected
010	KSV Map 2 selected
011	KSV Map 3 selected
100	KSV Map 4 selected
101	Reserved
110	Reserved
111	Reserved

Table 210. KSV Byte Registers Location

KSV Byte Number	Register Name	Register Addresses[1]
0	KSV_BYTE_0[7:0]	0x80[7:0]
1	KSV_BYTE_1[7:0]	0x81[7:0]
2	KSV_BYTE_2[7:0]	0x82[7:0]
3	KSV_BYTE_3[7:0]	0x83[7:0]
4	KSV_BYTE_4[7:0]	0x84[7:0]
5	KSV_BYTE_5[7:0]	0x85[7:0]
6	KSV_BYTE_6[7:0]	0x86[7:0]
7	KSV_BYTE_7[7:0]	0x87[7:0]
8	KSV_BYTE_8[7:0]	0x88[7:0]
9	KSV_BYTE_9[7:0]	0x89[7:0]
10	KSV_BYTE_10[7:0]	0x8A[7:0]

KSV Byte Number	Register Name	Register Addresses[1]
11	KSV_BYTE_11[7:0]	0x8B[7:0]
12	KSV_BYTE_12[7:0]	0x8C[7:0]
13	KSV_BYTE_13[7:0]	0x8D[7:0]
14	KSV_BYTE_14[7:0]	0x8E[7:0]
15	KSV_BYTE_15[7:0]	0x8F[7:0]
16	KSV_BYTE_16[7:0]	0x90[7:0]
17	KSV_BYTE_17[7:0]	0x91[7:0]
18	KSV_BYTE_18[7:0]	0x92[7:0]
19	KSV_BYTE_19[7:0]	0x93[7:0]
20	KSV_BYTE_20[7:0]	0x94[7:0]
21	KSV_BYTE_21[7:0]	0x95[7:0]
22	KSV_BYTE_22[7:0]	0x96[7:0]
23	KSV_BYTE_23[7:0]	0x97[7:0]
24	KSV_BYTE_24[7:0]	0x98[7:0]
25	KSV_BYTE_25[7:0]	0x99[7:0]
26	KSV_BYTE_26[7:0]	0x9A[7:0]
27	KSV_BYTE_27[7:0]	0x9B[7:0]
28	KSV_BYTE_28[7:0]	0x9C[7:0]
29	KSV_BYTE_29[7:0]	0x9D[7:0]
30	KSV_BYTE_30[7:0]	0x9E[7:0]
31	KSV_BYTE_31[7:0]	0x9F[7:0]
32	KSV_BYTE_32[7:0]	0xA0[7:0]
33	KSV_BYTE_33[7:0]	0xA1[7:0]
34	KSV_BYTE_34[7:0]	0xA2[7:0]
35	KSV_BYTE_35[7:0]	0xA3[7:0]
36	KSV_BYTE_36[7:0]	0xA4[7:0]
37	KSV_BYTE_37[7:0]	0xA5[7:0]
38	KSV_BYTE_38[7:0]	0xA6[7:0]
39	KSV_BYTE_39[7:0]	0xA7[7:0]
40	KSV_BYTE_40[7:0]	0xA8[7:0]
41	KSV_BYTE_41[7:0]	0xA9[7:0]
42	KSV_BYTE_42[7:0]	0xAA[7:0]
43	KSV_BYTE_43[7:0]	0xAB[7:0]
44	KSV_BYTE_44[7:0]	0xAC[7:0]
45	KSV_BYTE_45[7:0]	0xAD[7:0]
46	KSV_BYTE_46[7:0]	0xAE[7:0]
47	KSV_BYTE_47[7:0]	0xAF[7:0]
48	KSV_BYTE_48[7:0]	0xB0[7:0]
49	KSV_BYTE_49[7:0]	0xB1[7:0]
50	KSV_BYTE_50[7:0]	0xB2[7:0]
51	KSV_BYTE_51[7:0]	0xB3[7:0]
52	KSV_BYTE_52[7:0]	0xB4[7:0]
53	KSV_BYTE_53[7:0]	0xB5[7:0]
54	KSV_BYTE_54[7:0]	0xB6[7:0]
55	KSV_BYTE_55[7:0]	0xB7[7:0]
56	KSV_BYTE_56[7:0]	0xB8[7:0]
57	KSV_BYTE_57[7:0]	0xB9[7:0]
58	KSV_BYTE_58[7:0]	0xBA[7:0]
59	KSV_BYTE_59[7:0]	0xBB[7:0]
60	KSV_BYTE_60[7:0]	0xBC[7:0]
61	KSV_BYTE_61[7:0]	0xBD[7:0]
62	KSV_BYTE_62[7:0]	0xBE[7:0]
63	KSV_BYTE_63[7:0]	0xBF[7:0]

KSV Byte Number	Register Name	Register Addresses[1]
64	KSV_BYTE_64[7:0]	0xC0[7:0]
65	KSV_BYTE_65[7:0]	0xC1[7:0]
66	KSV_BYTE_66[7:0]	0xC2[7:0]
67	KSV_BYTE_67[7:0]	0xC3[7:0]
68	KSV_BYTE_68[7:0]	0xC4[7:0]
69	KSV_BYTE_69[7:0]	0xC5[7:0]
70	KSV_BYTE_70[7:0]	0xC6[7:0]
71	KSV_BYTE_71[7:0]	0xC7[7:0]
72	KSV_BYTE_72[7:0]	0xC8[7:0]
73	KSV_BYTE_73[7:0]	0xC9[7:0]
74	KSV_BYTE_74[7:0]	0xCA[7:0]
75	KSV_BYTE_75[7:0]	0xCB[7:0]
76	KSV_BYTE_76[7:0]	0xCC[7:0]
77	KSV_BYTE_77[7:0]	0xCD[7:0]
78	KSV_BYTE_78[7:0]	0xCE[7:0]
79	KSV_BYTE_79[7:0]	0xCF[7:0]
80	KSV_BYTE_80[7:0]	0xD0[7:0]
81	KSV_BYTE_81[7:0]	0xD1[7:0]
82	KSV_BYTE_82[7:0]	0xD2[7:0]
83	KSV_BYTE_83[7:0]	0xD3[7:0]
84	KSV_BYTE_84[7:0]	0xD4[7:0]
85	KSV_BYTE_85[7:0]	0xD5[7:0]
86	KSV_BYTE_86[7:0]	0xD6[7:0]
87	KSV_BYTE_87[7:0]	0xD7[7:0]
88	KSV_BYTE_88[7:0]	0xD8[7:0]
89	KSV_BYTE_89[7:0]	0xD9[7:0]
90	KSV_BYTE_90[7:0]	0xDA[7:0]
91	KSV_BYTE_91[7:0]	0xDB[7:0]
92	KSV_BYTE_92[7:0]	0xDC[7:0]
93	KSV_BYTE_93[7:0]	0xDD[7:0]
94	KSV_BYTE_94[7:0]	0xDE[7:0]
95	KSV_BYTE_95[7:0]	0xDF[7:0]
96	KSV_BYTE_96[7:0]	0xE0[7:0]
97	KSV_BYTE_97[7:0]	0xE1[7:0]
98	KSV_BYTE_98[7:0]	0xE2[7:0]
99	KSV_BYTE_99[7:0]	0xE3[7:0]
100	KSV_BYTE_100[7:0]	0xE4[7:0]
101	KSV_BYTE_101[7:0]	0xE5[7:0]
102	KSV_BYTE_102[7:0]	0xE6[7:0]
103	KSV_BYTE_103[7:0]	0xE7[7:0]
104	KSV_BYTE_104[7:0]	0xE8[7:0]
105	KSV_BYTE_105[7:0]	0xE9[7:0]
106	KSV_BYTE_106[7:0]	0xEA[7:0]
107	KSV_BYTE_107[7:0]	0xEB[7:0]
108	KSV_BYTE_108[7:0]	0xEC[7:0]
109	KSV_BYTE_109[7:0]	0xED[7:0]
110	KSV_BYTE_110[7:0]	0xEE[7:0]
111	KSV_BYTE_111[7:0]	0xEF[7:0]
112	KSV_BYTE_112[7:0]	0xF0[7:0]
113	KSV_BYTE_113[7:0]	0xF1[7:0]
114	KSV_BYTE_114[7:0]	0xF2[7:0]
115	KSV_BYTE_115[7:0]	0xF3[7:0]
116	KSV_BYTE_116[7:0]	0xF4[7:0]

KSV Byte Number	Register Name	Register Addresses[1]
117	KSV_BYTE_117[7:0]	0xF5[7:0]
118	KSV_BYTE_118[7:0]	0xF6[7:0]
119	KSV_BYTE_119[7:0]	0xF7[7:0]
120	KSV_BYTE_120[7:0]	0xF8[7:0]
121	KSV_BYTE_121[7:0]	0xF9[7:0]
122	KSV_BYTE_122[7:0]	0xFA[7:0]
123	KSV_BYTE_123[7:0]	0xFB[7:0]
124	KSV_BYTE_124[7:0]	0xFC[7:0]
125	KSV_BYTE_125[7:0]	0xFD[7:0]
126	KSV_BYTE_126[7:0]	0xFE[7:0]
127	KSV_BYTE_127[7:0]	0xFF[7:0]

[1] All KSVs are located in the repeater map.

Table 211. Registers Location for SHA-1 Hash Value V'

Register Name	Function	Address Location[1]
SHA_A[31:0]	H0 part of SHA-1 hash value V'. Register also called (V'.H1)[2].	0x20[7:0]: SHA_A[7:0] 0x21[7:0]: SHA_A[15:8] 0x22[7:0]: SHA_A[23:16] 0x23[7:0]: SHA_A[31:24]
SHA_B[31:0]	H1 part of SHA-1 hash value V'. Register also called (V'.H1)[2].	0x24[7:0]: SHA_B[7:0] 0x25[7:0]: SHA_B[15:8] 0x26[7:0]: SHA_B[23:16] 0x27[7:0]: SHA_B[31:24]
SHA_C[31:0]	H2 part of SHA-1 hash value V'. Register also called (V'.H2)[2].	0x28[7:0]: SHA_C[7:0] 0x29[7:0]: SHA_C[15:8] 0x2A[7:0]: SHA_C[23:16] 0x2B[7:0]: SHA_C[31:24]
SHA_D[31:0]	H3 part of SHA-1 hash value V'. Register also called (V'.H3)[2].	0x2C[7:0]: SHA_D[7:0] 0x2D[7:0]: SHA_D[15:8] 0x2E[7:0]: SHA_D[23:16] 0x2F[7:0]: SHA_D[31:24]
SHA_E[31:0]	H4 part of SHA-1 hash value V'. Register also called (V'.H4)[2].	0x30[7:0]: SHA_E[7:0] 0x31[7:0]: SHA_E[15:8] 0x32[7:0]: SHA_E[23:16] 0x33[7:0]: SHA_E[31:24]

[1] All registers specified in Table 211 are located in the repeater map.
[2] Refer to HDCP protection system Standards.

INTERFACE TO DPP SECTION

The video data below 2.25 Gbps from the HDMI section is sent to the CP section via the DPP block. The video data output by the HDMI section is always in a 4:4:4 format with 36 bits per pixel. This is irrespective of the encoding format of the video data encapsulated in the HDMI/DVI stream input to the HDMI receiver section (that is, 4:2:2 or 4:4:4).

- If the HDMI section receives a stream with video encoded in a 4:4:4 format, it passes the video data to the DPP section.
- If the HDMI section receives a stream with video encoded in a 4:2:2 format (see Figure 26), the HDMI section upconverts the video data into a 4:4:4 format, according to the UP_CONVERSION_MODE bit, and passes the upconverted video data to the DPP section (see Figure 27).
- If the HDMI receiver receives video data with fewer than 12 bits used per channel, the valid bits are left-shifted on each component channel with zeroes padding the bit below the LSB, before being sent to the DPP section.
- If the HDMI receiver receives video data above 2.25 Gbps, data must be send directly to the video output formatter, bypassing the DPP and CP core, where it is output using two video buses running at half pixel clock frequency

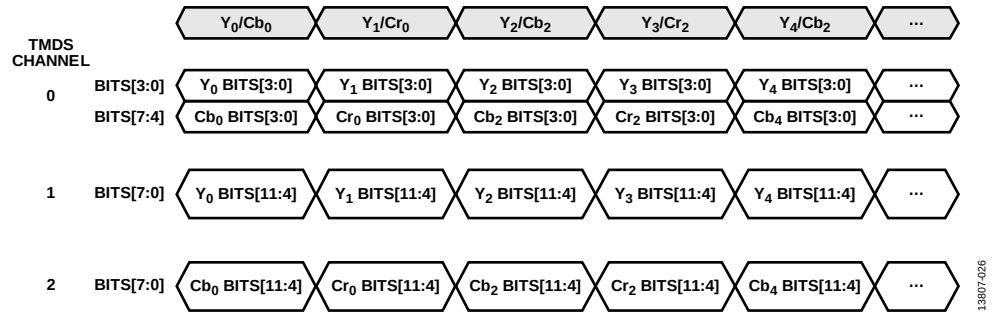


Figure 26. YCbCr 4:2:2 Video Data Encapsulated in HDMI Stream

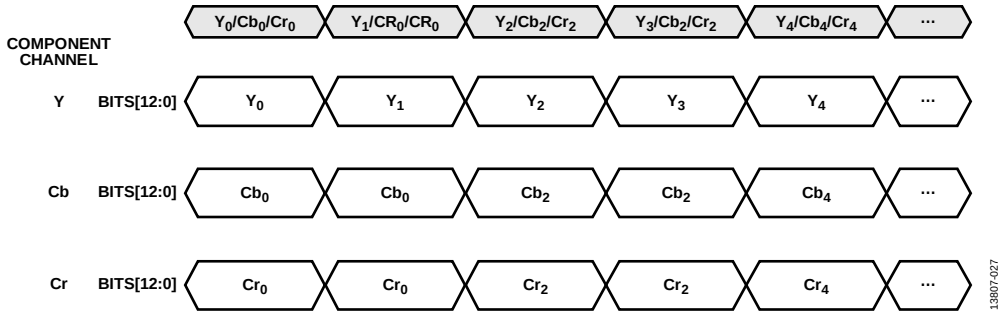


Figure 27. Video Stream Output by HDMI Core for YCbCr 4:2:2 Input and UP_CONVERSION = 0

UP_CONVERSION_MODE, Address 68 (HDMI), Address 0x1D[5]

This bit is a control to select linear or interpolated 4:2:2 to 4:4:4 conversion. A 4:2:2 incoming stream is upconverted to a 4:4:4 stream before being sent to the CP.

Table 212. UP_CONVERSION_MODE Function Description

UP_CONVERSION_MODE	Description
0 (default)	Cr and Cb samples are repeated in their respective channel
1	Interpolate Cr and Cb values

Note that when the ADV7613 pixel output format is set to 4:2:2, the DPP section downconverts the 4:4:4 stream from the HDMI section according to DS_WITHOUT_FILTER.

For a 4:4:4 HDMI input stream to the ADV7613, the DPP section filters and downsamples the video data from 4:4:4 to 4:2:2 format if DS_WITHOUT_FILTER is set to 0. The DPP section only downsamples, without filtering, the video data from the HDMI section if DS_WITHOUT_FILTER is set to 1.

For a 4:2:2 HDMI input stream, the functionality of DS_WITHOUT_FILTER is reversed. This inversion ensures that for a 4:2:2 HDMI input stream no filtering is applied if DS_WITHOUT_FILTER is left to its default value of 0. When a 4:2:2 HDMI input stream is input to the ADV7613, the DPP section downsamples, without filtering, the video data from 4:4:4 to 4:2:2 format if DS_WITHOUT_FILTER is set to 0. If DS_WITHOUT_FILTER is set to 1, the DPP filters and downsamples the video data from 4:4:4 to 4:2:2 format.

DS_WITHOUT_FILTER, Address 40 (IO), Address 0xE0[7]

This bit disables the chroma filters on Channel B and Channel C while keeping the downsampler functional.

Table 213. DS_WITHOUT_FILTER Function Description

DS_WITHOUT_FILTER	Description
0 (default)	Filters and downsamples
1	Downsamples only (no filtering)

COLOR SPACE INFORMATION SENT TO THE DPP AND CP SECTIONS

The HDMI section sends information regarding the color space of the video it outputs to the DPP and the CP sections. This color space information is derived from the DVI/HDMI status of the input stream the HDMI stection processes and from the AVI InfoFrame that the HDMI section decodes from the input stream.

The color space information sent by the HDMI section to the DDP and CP sections can be read via HDMI_COLORSPACE[3:0].

HDMI_COLORSPACE[3:0], Address 68 (HDMI), Address 0x53[3:0] (Read Only)

HDMI_COLORSPACE[3:0] is a readback of the HDMI input color space decoded from several fields in the AVI InfoFrame.

Table 214. HDMI_COLORSPACE[3:0] Function Description

HDMI_COLORSPACE[3:0]	Description
0000 (default)	RGB_LIMITED
0001	RGB_FULL
0010	YUV_601
0011	YUV_709
0100	XVYCC_601
0101	XVYCC_709
0110	YUV_601_FULL
0111	YUV_709_FULL
1000	sYCC 601
1001	Adobe YCC 601
1010	Adobe RGB

STATUS REGISTERS

Many status bit are available throughout the IO and HDMI maps. These status bits are listed in Table 215 to Table 224.

Table 215. HDMI Flags in IO Map Register 0x60

Bit Name	Bit Position	Description
AVI_INFO_RAW	0 (LSB)	Returns 1 if an AVI InfoFrame was received within last seven VSYNCs. For additional information, see the Interrupt Architecture Overview section.
AUDIO_INFO_RAW	1	Returns 1 if an AVI InfoFrame was received within last three VSYNCs. For additional information, see the Audio InfoFrame Registers section.
SPD_INFO_RAW	2	Returns 1 if a source product descriptor InfoFrame has been received. For additional information, see the SPD InfoFrame Registers section.
MS_INFO_RAW	3	Returns 1 if a MPEG InfoFrame was received within the last three VSYNCs. For additional information, see the MPEG Source InfoFrame Registers section.
VS_INFO_RAW	4	Returns 1 if a vendor specific InfoFrame has been received. For additional information, see the Vendor Specific InfoFrame Registers section.
ACP_PCKT_RAW	5	Returns 1 if an ACP packet was received within last 600 ms. For additional information, see the ACP Packet Registers section.
ISRC1_PCKT_RAW	6	Returns 1 if an ISRC1 packet was received. For additional information, see the ISRC Packet Registers section.
ISRC2_PCKT_RAW	7 (MSB)	Returns 1 if an ISRC2 packet was received. For additional information, see the ISRC Packet Registers section.

Table 216. HDMI Flags in IO Map Register 0x65

Bit Name	Bit Position	Description
GAMUT_MDATA_RAW	0 (LSB)	Returns 1 if a gamut metadata packet was received.
AUDIO_C_PCKT_RAW	1	Returns 1 if an audio clock regeneration packet has been received. Reset to 0 following a packet detection flag reset condition.
GEN_CTL_PCKT_RAW	2	Returns 1 if general control packet has been received. Reset to 0 following a packet detection flag reset condition.
HDMI_MODE_RAW	3	Returns 1 if a HDMI stream is being received. For additional information, see HDMI/DVI Status Bits section.
AUDIO_CH_MD_RAW	4	Returns 1 if the audio channel mode is multichannel (2-, 4-, 6-, or 8-channel) audio. Reset to 0 following a packet detection flag reset condition. For additional information, see the Audio Channel Mode section.
AV_MUTE_RAW	5	Returns 1 if the latest general control packet received has AV_MUTE asserted. Reset to 0 following packet detection flag reset condition.
INTERNAL_MUTE_RAW	6	Returns 1 if ADV7613 has internally muted the audio data. For additional information, see the Internal Mute Status section.
CS_DATA_VALID_RAW	7 (MSB)	Returns 1 if channel status bit readback registers in HDMI map, Address 0x36 to 0x3A are valid. For additional information, see the Validity Status Flag section.

Table 217. HDMI Flags in IO Map Register 0x6A

Bit Name	Bit Position	Description
DE_REGEN_LCK_RAW	0 (LSB)	Description available in the Primary Port Horizontal Filter Measurements section.
V_LOCKED_RAW	1	Description available in the Primary Port Horizontal Filter Measurements section.
VIDEO_3D_RAW	2	Raw interrupt status of 3D video detection flag (refer to VIDEO_3D_ST in Table 384).
TMDS_CLK_A_RAW	4	Description available in the TMDS Clock Activity Detection section
TMDSPLL_LCK_A_RAW	6	Description available in the TMDS Measurement After TMDS PLL section

Table 218. HDMI Flags in IO Map Register 0x6F

Bit Name	Bit Position	Description
CABLE_DET_A_RAW	0	Description available in the +5 V Cable Detect section.
HDMI_ENCRPT_A_RAW	2	Description available in the HDCP Decryption Engine section.

Table 219. HDMI Flags in IO Map Register 0x79

Bit Name	Bit Position
NEW_AVI_INFO_RAW	0 (LSB)
NEW_AUDIO_INFO_RAW	1
NEW_SPD_INFO_RAW	2
NEW_MS_INFO_RAW	3
NEW_VS_INFO_RAW	4
NEW_ACP_PCKT_RAW	5
NEW_ISRC1_PCKT_RAW	6
NEW_ISRC2_PCKT_RAW	7 (MSB)

Table 220. HDMI Flags in IO Map Register 0x7E

Bit Name	Bit Position	Description
NEW_GAMUT_MDATA_RAW	0 (LSB)	When set to 1 indicates that a gamut metadata packet with new content has been received. Once set, this bit remains high until the interrupt is cleared via NEW_GAMUT_MDATA_PCKT_CLR (IO Map 0x80[0]).
AUDIO_PCKT_ERR_RAW	1	When set to 1 indicates that an uncorrectable error was detected in the body of an audio packet. Once set, this bit remains high until the interrupt is cleared via AUDIO_PCKT_ERR_CLR (IO Map 0x80[1]).
PACKET_ERROR_RAW	2	When set to 1 it indicates an uncorrectable EEC error was detected in the body or header of any packet. Once set, this bit remains high until the interrupt is cleared via PACKET_ERROR_CLR (IO Map 0x80[2]).
CHANGE_N_RAW	3	When set to 1 it indicates the N value of the ACR packets has changed. Once set, this bit remains high until the interrupt is cleared via CHANGE_N_CLR (IO Map 0x80 [3]).
CTS_PASS_THRSH_RAW	4	When set to 1 it indicates the CTS value of the ACR packets has exceeded the threshold set by CTS_CHANGE_THRESHOLD. Once set, this bit remains high until the interrupt is cleared via CTS_PASS_THRSH_CLR (IO Map 0x80[4]).
FIFO_OVERFLO_RAW	5	When set to 1 it indicates the audio FIFO write pointer has reached the read pointer causing the audio FIFO to overflow. Once set, this bit remains high until the interrupt is cleared via FIFO_OVERFLO_CLR (IO Map 0x80[5]).
FIFO_UNDERFLO_RAW	6	When set to 1 it indicates the audio FIFO read pointer has reached the write pointer causing the audio FIFO to underflow. Once set, this bit remains high until the interrupt is cleared via FIFO_UNDERFLO_CLR (IO Map 0x80[6]).
FIFO_NEAR_OVFL_RAW	7 (MSB)	When set to 1 it indicates the audio FIFO is near overflow as the number FIFO registers containing stereo data is greater or equal to value set in AUDIO_FIFO_ALMOST_FULL_ THRESHOLD. Once set, this bit remains high until the interrupt is cleared via FIFO_NEAR_OVFL_CLR (IO Map 0x80[7]).

Table 221. HDMI Flags in IO Map Register 0x83

Bit Name	Bit Position	Description
FIFO_NEAR_UFLO_RAW	0 (LSB)	When set to 1 it indicates the audio FIFO is near underflow as the number of FIFO registers containing stereo data is less or equal to value set in AUDIO_FIFO_ALMOST_EMPTY_ THRESHOLD. Once set, this bit remains high until the interrupt is cleared via FIFO_NEAR_UFLO_CLR (IO Map 0x85[0]).
NEW_TMDS_FRQ_RAW	1	When set to 1 it indicates the TMDS frequency has changed by more than the tolerance set in FREQTOLERANCE[3:0] Once set, this bit remains high until the interrupt is cleared via NEW_TMDS_FREQ_CLR (IO Map 0x85[1]).
AUDIO_FLT_LINE_RAW	2	When set to 1 it indicates audio sample packet has been received with the flat line bit set to 1. Once set, this bit remains high until the interrupt is cleared via AUDIO_FLT_LINE_CLR (IO Map 0x85[2]).
NEW_SAMP_RT_RAW	3	When set to 1 it indicates that audio sampling frequency field in channel status data has changed. Once set, this bit remains high until the interrupt is cleared via NEW_SAMP_ RT_CLR (IO Map 0x85[3]).
PARITY_ERROR_RAW	4	When set to 1 it indicates an audio sample packet has been received with parity error. Once set, this bit remains high until the interrupt is cleared via PARITY_ERROR_CLR (IO Map 0x85 [4]).
AUDIO_MODE_CHNG_RAW	5	When set to 1 it indicates that the type of audio packet received has changed. The following are considered audio modes, no audio, PCM, DSD, HBR, or DST. AUDIO_SAMPL_PCKT_DET, DSD_PACKET_DET, DST_AUDIO_PCKT_DET, and HBR_AUDIO_PCKT_DET used identify type of audio packet currently received. Once set, this bit remains high until the interrupt is cleared via AUDIO_MODE_CHNG_CLR (IO Map 0x85[5]).
VCLK_CHNG_RAW	6	When set to 1 it indicates that irregular or missing pulses are detected in the TMDS clock. Once set, this bit remains high until the interrupt is cleared via VCLK_CHNG_CLR (IO Map 0x85[6]).
DEEP_COLOR_CHNG_RAW	7 (MSB)	When set to 1 it indicates a change in the deep color mode has been detected. Once set, this bit remains high until the interrupt is cleared via DEEP_COLOR_CHNG_CLR (IO Map 0x85[7]).

Table 222. HDMI InfoFrame Checksum Error Flags in IO Map

Bit Name	IO Map Location	Description
AVI_INF_CKS_ERR_RAW	0x88[4]	Description available in the InfoFrame Checksum Error Flags section.
AUD_INF_CKS_ERR_RAW	0x88[5]	Description available in the InfoFrame Checksum Error Flags section.
SPD_INF_CKS_ERR_RAW	0x88[6]	Description available in the InfoFrame Checksum Error Flags section.
MS_INF_CKS_ERR_RAW	0x88[7]	Description available in the InfoFrame Checksum Error Flags section.
VS_INF_CKS_ERR_RAW	0x8D[0]	Description available in the InfoFrame Checksum Error Flags section.

Table 223. AKSV Update Flags and RI Expired Flag in IO Map Register 0x88

Bit Name	Bit Position	Description
AKSV_UPDATE_A_RAW	0	When set to 1 it indicates that transmitter has written its AKSV into HDCP registers for Port A. When set, this bit remains high until the interrupt is cleared via AKSV_UPDATE_A_CLR (IO Map, Address 0x8A[0]).
RI_EXPIRED_A_RAW	2	Status of Port A Ri expired interrupt signal. When set to 1, it indicates that HDCP cipher Ri value for Port A is expired. Once set, this bit remains high until it is cleared via RI_EXPIRED_A_CLR (HDMI map, Address 0x8A[2]).

Table 224. HDMI Flags in HDMI Map

Bit Name	HDMI Map Location	Description
AUDIO_PLL_LOCKED	0x04[0]	Description available in the Locking Mechanism section.
AUDIO_SAMPLE_PCKT_DET	0x18[0]	Description available in the Audio Packet Type Flags section.
DSD_PACKET_DET	0x18[1]	Description available in the Audio Packet Type Flags section.
DST_AUDIO_PCKT_DET	0x18[2]	Description available in the Audio Packet Type Flags section.
HBR_AUDIO_PCKT_DET	0x18[3]	Description available in the Audio Packet Type Flags section.
DCFIFO_LOCKED	0x1C[3]	Description available in the Video FIFO section.

HDMI SECTION RESET STRATEGY

The reset strategy implemented for the HDMI section is as follows.

A global chip reset is triggered by asserting the reset pin to a low level. The HDMI section, excluding the EDID/repeater controller, is reset when a global reset is triggered.

A loss of TMDS clock or 5 V signal on the HDMI port selected via HDMI_PORT_SELECT resets the entire HDMI section except for the EDID/repeater controller and the audio section.

The loss of a 5 V signal condition is discarded if DIS_CABLE_DET_RST is set high.

For a DVI mode reset, the packet processing block, including InfoFrame memory is held in reset when the HDMI section processes a DVI stream.

For a EDID/repeater controller reset, the EDID/repeater controller is reset when the DVDD supplies go low or when HDCP_REPT_EDID_RESET is set high.

HDMI PACKET DETECTION FLAG RESET

A packet detection flag reset is triggered when any of the following events occur:

- The ADV7613 is powered up.
- The ADV7613 is reset.
- A TMDS clock is detected, after a period of no clock activity, on the selected HDMI port.
- The selected HDMI port is changed.

The signal from the 5 V input pin of the HDMI port selected through HDMI_PORT_SELECT transitions to a high. This condition is discarded if DIS_CABLE_DET_RST is set high.

DATA PREPROCESSOR, COLOR SPACE CONVERSION, AND COLOR CONTROLS

COLOR SPACE CONVERSION MATRIX

The ADV7613 provides any-to-any color space support. It supports formats such as RGB, YUV, YCbCr, and many other color spaces. The data preprocessor (DPP) and component processor (CP) run at speeds of up to 170 MHz. The ADV7613 features a 3×3 color space conversion matrix (CSC) in the CP block (CP CSC), as shown in Figure 28. The CP CSC also provides color controls for brightness, contrast, saturation, and hue adjustments. The DPP block features an automatic CSC. The ADV7613 automatically configures the DPP CSC depending on the input and output formats and the use of the color control feature.

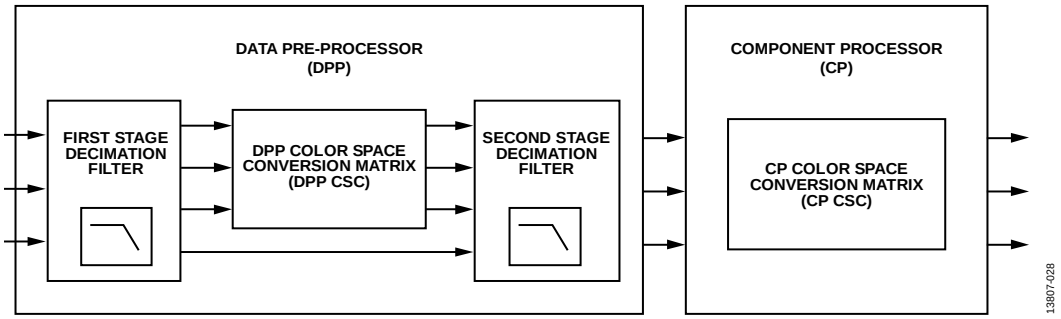


Figure 28. DPP/CP CSC Block Diagram

The configuration of the color space conversion using the CP CSC block and a description of the adjustable register bits are provided in Figure 29.

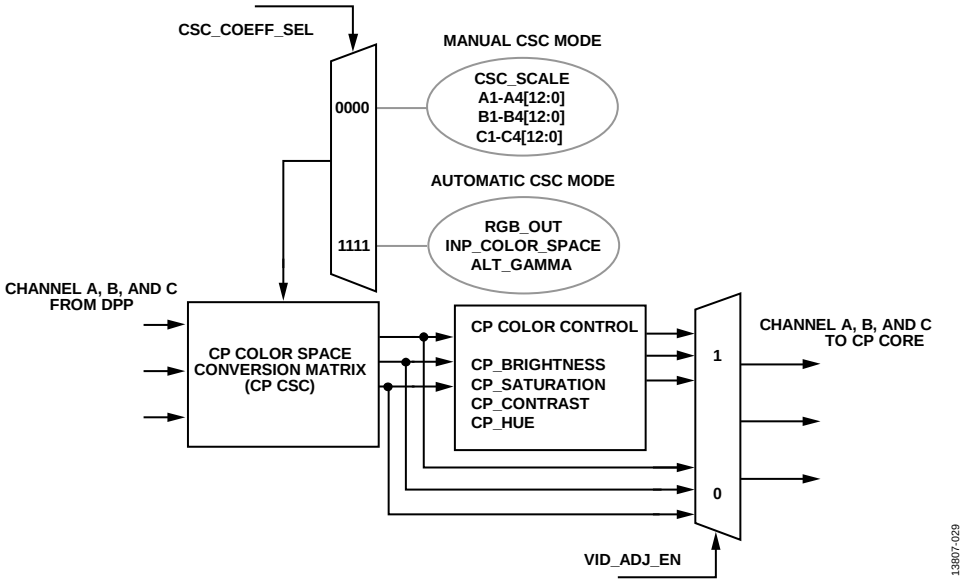


Figure 29. Configuring CP CSC Block

CP CSC Selection

MAN_CP_CSC_EN, Address 44 (CP), Address 0x69[4]

MAN_CP_CSC_EN is a control to manually enable the CP CSC. By default, the CP CSC is automatically enabled if either a color-space conversion or video adjustments (hue, saturation, contrast, brightness) are determined to be required due to other I²C settings. If MAN_CP_CSC_EN is set to 1, the CP CSC is forced into the enabled state.

Table 225. MAN_CP_CSC_EN Function Description

MAN_CP_CSC_EN	Description
0 (default)	CP CSC is automatically enabled if required, for example, if either a color space conversion or video adjustment (hue, saturation, contrast, brightness) is determined to be required due to other I²C settings.
1	Manual override to force CP CSC to be enabled.

Selecting Automatic or Manual CP CSC Conversion Mode

The ADV7613 CP CSC provides two modes for the CSC configuration: automatic CSC mode and manual CSC mode.

In automatic CSC mode, the user is required to program the input color space and the output color space for the correct operation of the CSC matrix. Manual CSC mode allows the user to program all the color space conversion by manually programming CSC coefficients.

CSC_COEFF_SEL[3:0], Address 44 (CP), Address 0x68[7:4]

CSC_COEFF_SEL[3:0] is a control to select the mode the CP CSC operates in.

Table 226. CSC_COEFF_SEL[3:0] Function Description

CSC_COEFF_SEL[3:0]	Description
0000	CP CSC configuration in manual mode
1111 (default)	CP CSC configured in automatic mode
xxxx	Reserved

The selection of the CSC is automated in the ADV7613. Automatic or manual CSC mode can be selected by setting the CSC_COEFF_SEL[3:0] bits. When CSC_COEFF_SEL[3:0] is set to 0b1111, the CSC mode is automatically selected, based on the input color space and output color space required and set through the INP_COLOR_SPACE[3:0], RGB_OUT, and ALT_GAMMA registers.

Automatic Color Space Conversion Matrix

The CSC matrix, automatic gain control (AGC) target gain values, and offset values can be configured automatically via the INP_COLOR_SPACE[3:0], RGB_OUT, ALT_GAMMA, and OP_656_RANGE_SEL registers.

INP_COLOR_SPACE[3:0], IO, Address 0x02[7:4]

INP_COLOR_SPACE[3:0] is a control to set the color space of the input video. It is used in conjunction with ALT_GAMMA and RGB_OUT to configure the color space converter. A value of 4'b1111 selects automatic setting of the input color space based on the primary mode and video standard settings. Setting 1000 to Setting 1110 are undefined.

Table 227. INP_COLOR_SPACE[3:0] Function Description

INP_COLOR_SPACE[3:0]	Description
0000	Forces RGB (range 16 to 235) input
0001	Forces RGB (range 0 to 255) input
0010	Forces YCrCb input (601 color space) (range 16 to 235)
0011	Forces YCrCb input (709 color space) (range 16 to 235)
0100	Forces XVYCC 601
0101	Forces XVYCC 709
0110	Forces YCrCb input (601 color space) (range 0 to 255)
0111	Forces YCrCb input (709 color space) (range 0 to 255)
1111 (default)	Input color space depends on color space reported by HDMI block.

Table 228. Automatic Input Color Space Selection

PRIM_MODE[3:0]	VID_STD[5:0]	Input Color Space	Input Range	Comments
0101	xxxx	Dependent on AVI InfoFrame	0:255 for YUV Dependent on AVI InfoFrame for RGB	HDMI component modes
0110	xxxx	Dependent on AVI InfoFrame	0:255 for YUV Dependent on AVI InfoFrame for RGB	HDMI graphic modes

RGB_OUT, IO, Address 0x02[1]

RGB_OUT is a control to select output color space and the correct digital blank level and offsets on the RGB or YPrPb outputs. It is used in conjunction with the INP_COLOR_SPACE[3:0] and ALT_GAMMA bits to select the applied CSC.

Table 229. RGB_OUT Function Description

RGB_OUT	Description
0 (default)	YPbPr color space output
1	RGB color space output

ALT_GAMMA, IO, Address 0x02[3]

ALT_GAMMA is a control to set the color space of the input video. It is used in conjunction with ALT_GAMMA and RGB_OUT to configure the color space converter. A value of 4'b1111 selects automatic setting of the input color space based on the primary mode and video standard settings. Setting 1000 to Setting 1110 are undefined.

Table 230. ALT_GAMMA Function Description

ALT_GAMMA	Description
0 (default)	No conversion.
1	YUV601 to YUV709 conversion applied if input is YUV601. YUV709 to YUV601 conversion applied if input is YUV709.

Table 231. Automatic CSC Selection

		CSC Mode Used (Output)	
INP_COLOR_SPACE[3:0] (Input Color Space)	RGB_OUT	ALT_GAMMA = 0	ALT_GAMMA = 1
00 = RGB	0	YCbCr 601	YCbCr 709
	1	RGB	RGB
01 = (YCbCr /YUV 601)	0	YCbCr 601	YCbCr 709
	1	RGB	RGB
10 = (YCbCr /YUV 709)	0	YCbCr 709	YCbCr 601
	1	RGB	RGB

CSC_COEFF_SEL_RB[3:0], Address 44 (CP), Address 0xF4[7:4] (Read Only)

CSC_COEFF_SEL_RB[3:0] is the readback of the CP CSC conversion when configured in automatic mode.

Table 232. CSC_COEFF_SEL_RB[3:0] Function Description

CSC_COEFF_SEL_RB[3:0]	Description
0000 (default)	CSC is bypassed
0001	YPbPr 601 to RGB
0011	YPbPr 709 to RGB
0101	RGB to YPbPr 601
0111	RGB to YPbPr 709
1001	YPbPr 709 to YPbPr 601
1010	YPbPr 601 to YPbPr 709
1111	CSC in manual mode
xxxx	Reserved

Table 233. CSC Configuration for All CSC Modes Reported by CSC_COEFF_SEL_RB

CSC Mode	CSC_SCALE [1:0]	A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4
0b0000	CSC in bypass mode. In this mode the CSC effectively performs a color conversion based on the CSC coefficients set in registers CSC_SCALE, A1, A2, A3, A4, B1, B2, B3, B4, C1, C2, C3, and C4.												
0b0001	0b01	0x0800	0x1A6A	0x1D50	0x0423	0x0800	0x0AF8	0x0000	0x1A84	0x0800	0x0000	0x0DDB	0x1912
0b0011	0b01	0x0800	0x1C54	0x1E89	0x0291	0x0800	0x0C52	0x0000	0x19D7	0x0800	0x0000	0x0E87	0x18BC
0b0101	0b00	0x0964	0x04C9	0x01D3	0x0000	0x1927	0x082D	0x1EAC	0x0800	0x1A93	0x1D3F	0x082D	0x0800
0b0111	0b00	0x0B71	0x0368	0x0127	0x0000	0x1893	0x082D	0x1F3F	0x0800	0x19B2	0x1E21	0x082D	0x0800
0b1001	0b01	0x0800	0x0188	0x00CB	0x1ED7	0x0000	0x07DE	0x1F6C	0x005B	0x0000	0x1F1D	0x07EB	0x007B
0b1010	0b01	0x0800	0x1E56	0x1F14	0x014A	0x0000	0x0834	0x009A	0x1F9A	0x0000	0x00EB	0x0826	0x1F78

HDMI Automatic CSC Operation

In HDMI mode, the ADV7613 provides an automatic CSC function based on the AVI InfoFrame sent from the source. The flowchart in Figure 30 shows the mechanism of the ADV7613 automatic CSC functionality in HDMI mode.

Note that in the following flowcharts, a dashed line represents a state that is undefined according to the CEA-861D specification, and therefore must never happen. In the event that it does somehow occur, the ADV7613 retains the previous colorimetry.

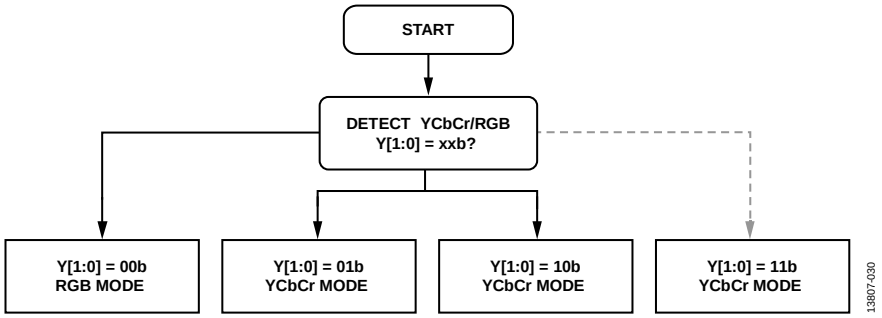


Figure 30. HDMI Automatic CSC Flowchart

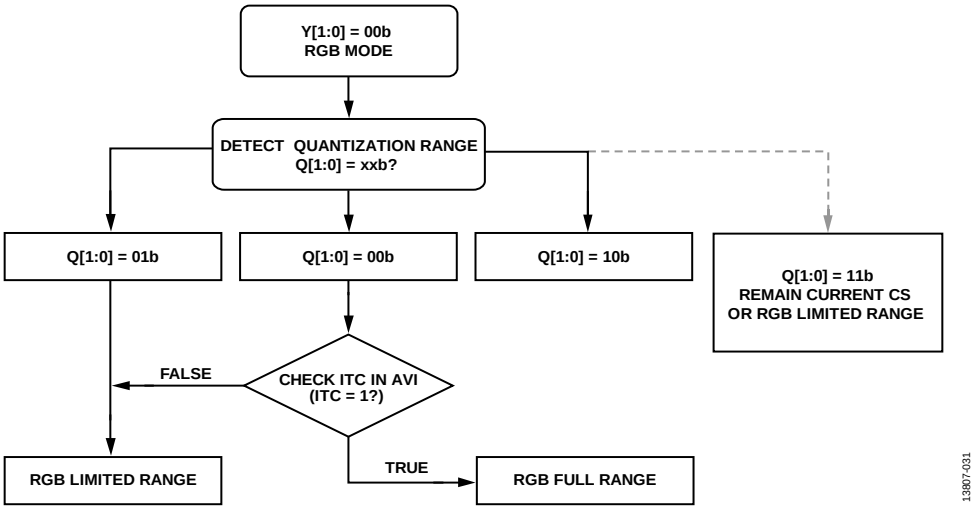


Figure 31. HDMI Automatic CSC Flowchart (Case RGB)

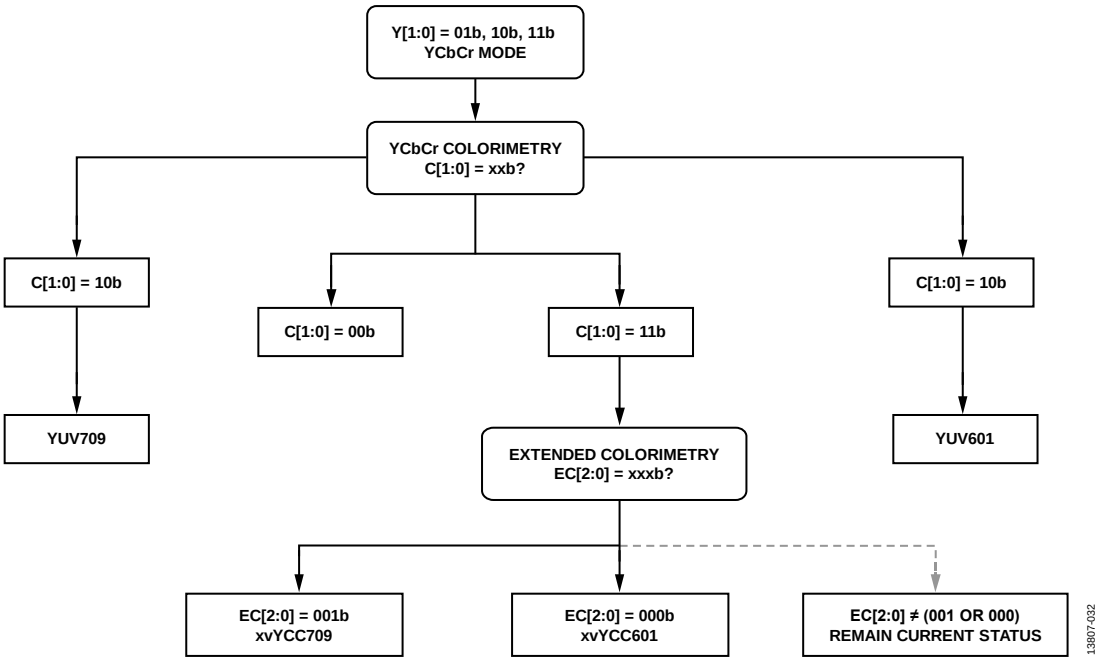


Figure 32. HDMI Automatic CSC Flowchart (Case YCbCr-1)

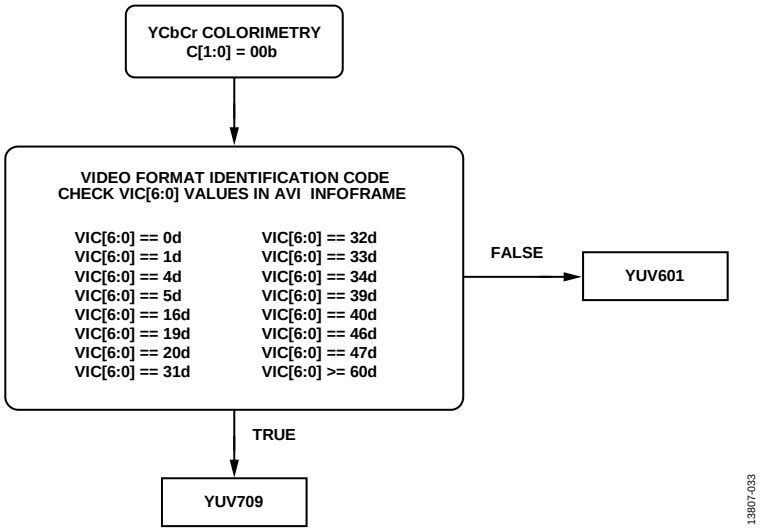


Figure 33. HDMI Automatic CSC Flowchart (Case YCbCr-2)

In the RGB case (see Figure 34), the ADV7613 has the programmability to control manually the RGB limited/full range regardless of the ITC bit.

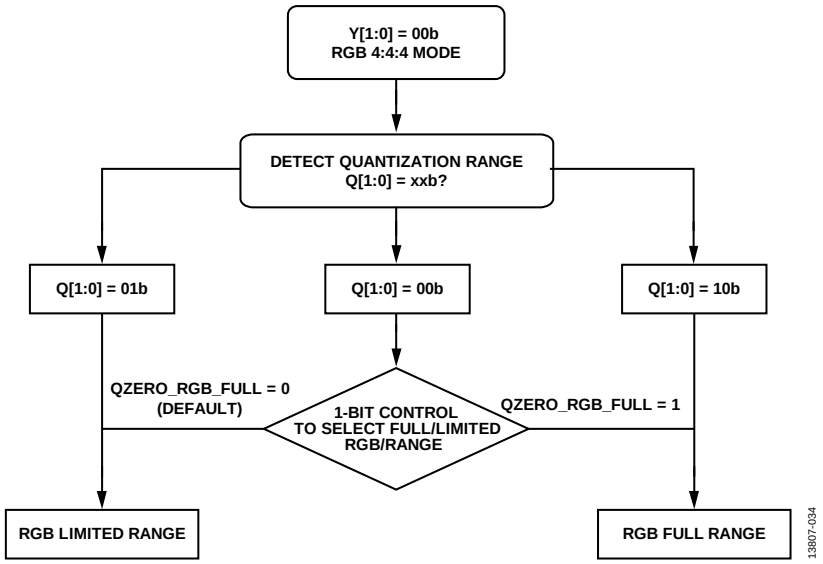


Figure 34. Manual RGB Range Control Flowchart for Automatic CSC (Case RGB)

QZERO_ITC_DIS, Address 68 (HDMI), Address 0x47[2]

QZERO_ITC_DIS is a control to select manual control of the RGB colorimetry when the AVI InfoFrame field Q[1:0] = 00. It is used in conjunction with QZERO_RGB_FULL.

Table 234. QZERO_ITC_DIS Function Description

QZERO_ITC_DIS	Description
0 (default)	AVI InfoFrame ITC bit decides RGB-full or limited range in case Q[1:0] = 00
1	Manual RGB range as per QZERO_RGB_FULL

QZERO_RGB_FULL, Address 68 (HDMI), Address 0x47[1]

QZERO_RGB_FULL is a control to manually select the HDMI colorimetry when AVI InfoFrame field Q[1:0] = 00. It is valid only when QZERO_ITC_DIS is set to 1.

Table 235. QZERO_RGB_FULL Function Description

QZERO_RGB_FULL	Description
0 (default)	RGB-limited range when Q[1:0] = 00
1	RGB-full when Q[1:0] = 00

Manual Color Space Conversion Matrix

The CP CSC matrix in the ADV7613 is a 3 × 3 matrix with full programmability of all coefficients in the matrix in manual mode. Each coefficient is 12 bits wide to ensure signal integrity is maintained in the CP CSC section. The CP CSC contains three identical processing channels, one of which is shown in Figure 35. The main inputs labeled In_A, In_B, and In_C come from the 36-bit digital input from the HDMI section. Each input to the individual channels to the CSC is multiplied by a separate coefficient for each channel.

In Figure 35, these coefficients are marked A1, A2 and A3. The variable labeled A4 is used as an offset control for Channel A in the CSC. There is also a further CP CSC control bit labeled CSC_SCALE[1:0]; this control can be used to accommodate coefficients that extend the supported range. The functional diagram for a single channel in the CP CSC as per Figure 35 is repeated for the other two remaining channels, Channel B and Channel C. The coefficients for these channels are called B1, B2, B3, B4, C1, C2, C3, and C4.

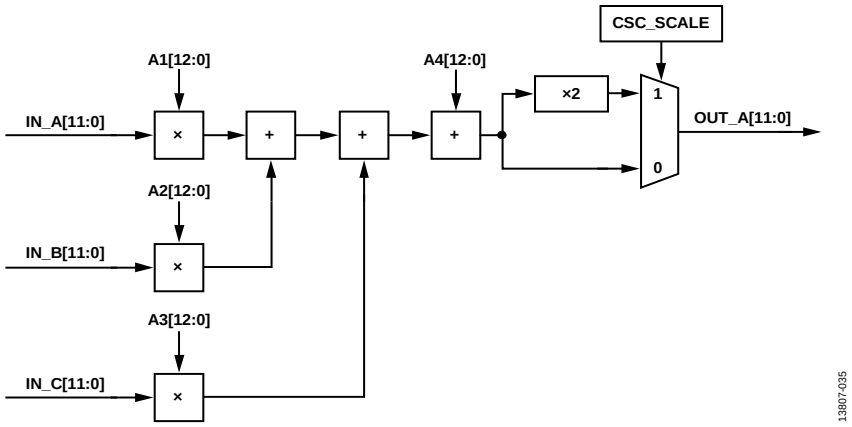


Figure 35. Single CSC Channel

The coefficients mentioned previously are detailed in Table 236 along with the default values for these coefficients.

Table 236. CSC Coefficients

Function Bit	CP Map Address	Reset Value (Hex)	Description
A1[12:0]	0x57[4:0], 0x58[7:0]	0x800	Coefficient for Channel A
A2[12:0]	0x55[1:0], 0x56[7:0], 0x57[7:5]	0x000	Coefficient for Channel A
A3[12:0]	0x54[6:0], 0x55[7:2]	0x000	Coefficient for Channel A
B1[12:0]	0x5E[4:0], 0x5F[7:0]	0x000	Coefficient for Channel B
B2[12:0]	0x5C[1:0], 0x5D[7:0], 0x5E[7:5]	0x800	Coefficient for Channel B
B3[12:0]	0x5B[6:0], 0x5C[7:2]	0x000	Coefficient for Channel B
C1[12:0]	0x65[4:0], 0x66[7:0]	0x000	Coefficient for Channel C
C2[12:0]	0x63[1:0], 0x64[7:0], 0x65[7:5]	0x000	Coefficient for Channel C
C3[12:0]	0x62[6:0], 0x63[7:2]	0x800	Coefficient for Channel C
CSC_SCALE[1:0]	0x52[7:6]	0x01	Scaling for CSC formula
A4[12:0]	0x52[4:0], 0x53[7:0]	0x000	Offset for Channel A
B4[12:0]	0x59[4:0], 0x5A[7:0]	0x000	Offset for Channel B
C4[12:0]	0x60[4:0], 0x61[7:0]	0x000	Offset for Channel C

CSC_SCALE[1:0], Address 44 (CP), Address 0x52[7:6]

CSC_SCALE[1:0] is a control to set the CSC coefficient scaler.

Table 237. CSC_SCALE[1:0] Function Description

CSC_SCALE[1:0]	Description
00	CSC scaler set to 1.
01 (default)	CSC scaler set to 2.
10	Reserved. Do not use.
11	Reserved. Do not use.

CSC Manual Programming

The equations performed by the CP CSC are as follows.

For CSC Channel A,

$$Out\_A = \left[In\_A \times \frac{A1[12:0]}{4096} + In\_B \times \frac{A2[12:0]}{4096} + In\_C \times \frac{A3[12:0]}{4096} + A4[12:0] \right] \times 2^{CSC\_SCALE} \quad (4)$$

For CSC Channel B,

$$Out\_B = \left[In\_A \times \frac{B1[12:0]}{4096} + In\_B \times \frac{B2[12:0]}{4096} + In\_C \times \frac{B3[12:0]}{4096} + B4[12:0] \right] \times 2^{CSC\_SCALE} \quad (5)$$

For CSC Channel C,

$$Out\_C = \left[In\_A \times \frac{C1[12:0]}{4096} + In\_B \times \frac{C2[12:0]}{4096} + In\_C \times \frac{C3[12:0]}{4096} + C4[12:0] \right] \times 2^{CSC\_SCALE} \quad (6)$$

As can be seen from Equation 4, Equation 5, and Equation 6, the A1, A2, A3; B1, B2, B3, and C1, C2, C3 coefficients are used to scale the primary inputs. The values of A4, B4, and C4 are added as offsets. The CSC_SCALE[1:0] bits allow the user to implement a conversion formula in which the coefficients exceed the standard range of [−4095/4096 ... 4095/4096]. The overall range of the CSC is [0 … 1] for unipolar signals (for example, Y, R, G, and B) and [−0.5 … +0.5] for bipolar signals (for example, Pr and Pb).

Note that the bipolar signals must be offset to midrange, for example, 2048.

To arrive at programming values from typical formulas, perform the following steps:

1. Determine the dynamic range of the equation. The dynamic range of the CSC is [0 … 1] or [−0.5 … +0.5]. Equations with a gain larger than 1 need to be scaled back. Errors in the gain can be compensated for in the gain stages of the follow on blocks.
2. Scale the equations, if necessary.
3. Check the value of each coefficient. The coefficients can only be programmed in the range [−0.99 … +0.99].
4. To support larger coefficients, use the CSC_SCALE[1:0] function.
5. Determine the setting for CSC_SCALE[1:0] and adjust coefficients, if necessary.
6. Program the coefficient values. Convert the float point coefficients into 12-bit fixed decimal format. Convert into binary format, using twos complement for negative values.
7. Program A1 to A3, B1 to B3, and C1 to C3.
8. Program the offset values. Depending on the type of CSC, offsets may have to be used.
9. Program A4, B4, and C4.

CSC Example

The following set of equations gives an example of a conversion from a gamma corrected RGB signal into a YCbCr color space signal.

$$Out\_A = \left[In\_A \times \frac{A1[12:0]}{4096} + In\_B \times \frac{A2[12:0]}{4096} + In\_C \times \frac{A3[12:0]}{4096} + A4[12:0] \right] \times 2^{CSC\_SCALE}$$

$$Out\_B = \left[In\_A \times \frac{B1[12:0]}{4096} + In\_B \times \frac{B2[12:0]}{4096} + In\_C \times \frac{B3[12:0]}{4096} + B4[12:0] \right] \times 2^{CSC\_SCALE}$$

$$Out\_C = \left[In\_A \times \frac{C1[12:0]}{4096} + In\_B \times \frac{C2[12:0]}{4096} + In\_C \times \frac{C3[12:0]}{4096} + C4[12:0] \right] \times 2^{CSC\_SCALE}$$

Note that the original equations give offset values of 128 for the Pr and Pb components. The value of 128 equates to half the range on an 8-bit system. It must be noted that the CSC operates on a 12-bit range. The offsets, therefore, must be changed from 128 to half the range of a 12-bit system, which equates to 2048.

The maximum range for each equation, that is, each output data path, can only be [0 ... 1] or [−0.5 ... +0.5]. Equations with a larger gain must be scaled back into range. The gain error can be compensated for in the gain stage of the follow on blocks.

The ranges of the three equations are shown in Table 238.

Table 238. Equation Ranges

Equation	Minimum Value	Maximum Value	Range
Y	0 + 0 + 0 = 0	0.59 + 0.3 + 0.11 = 1	[0 … 1] = 1
Pb	(−0.34) + (−0.17) = −0.51	0.51	[−0.51 …+ 0.51] = 1.02
Pr	(−0.43) + (−0.08) = −0.51	0.51	[−0.51 … +0.51] = 1.02

As can be seen from Table 238, the range for the Y component fits into the CSC operating range. However, the Pb and Pr ranges slightly exceed the range. To bring all equations back into the supported range, they must be scaled back by 1/1.02.

If equations fall outside the supported range, overflow or underflow can occur and undesirable wrap around effects (large number overflowing to small ones) can occur.

$$Y = \frac{0.59}{1.02} \times G + \frac{0.3}{1.02} \times R + \frac{0.11}{1.02} \times B = 0.58 \times G + 0.29 \times R + 0.11 \times B$$

$$Pb = \frac{-0.34}{1.02} \times G + \frac{-0.17}{1.02} \times R + \frac{0.51}{1.02} \times B + 2048 = -0.33 \times G - 0.17 \times R + 0.5 \times B + 2048$$

$$Pr = \frac{-0.43}{1.02} \times G + \frac{0.51}{1.02} \times R + \frac{-0.08}{1.02} \times B + 2048 = -0.42 \times G + 0.5 \times R - 0.08 \times B + 2048$$

Note that the scaling of the dynamic range does not affect the static offset.

Check the Value of Each Coefficient

The maximum value for each coefficient on its own can only be within the range of −4096/+4096 to 4095/4096, which equals [1 … +0.999755859375]. Values outside this range do not fit into the 12-bit fixed point format used to program the coefficients.

If the value of one or more coefficients after scaling of the overall equation exceeds the supported coefficient range, CSC_SCALE[1:0] must be set.

With CSC_SCALE[1:0] set high, all coefficients must be scaled by half, which makes them fit into the given coefficient range. The overall outputs of the CSC are gained up by a fixed value of two, thus compensating for the scaled down coefficients.

In the preceding example, each coefficient on its own is within the range of

$$\frac{-4095}{4096} \leq Coefficient \leq \frac{4095}{4096}$$

Therefore, all coefficients can be programmed directly and the CSC_SCALE[1:0] bit must be set to 0.

Note that, to achieve a coefficient value of 1.0 for any given coefficient, CSC_SCALE must be set high and the coefficient must actually be programmed to a value of 0.5. Otherwise, the largest value is 4095/4096 = 0.9997, which is not exactly 1. Although this value can be interpreted as a 1, it is recommended to use the value of 0.5 and the CSC_SCALE bit for maximum accuracy.

For very large coefficient values (for example, 2.58), use a combination of CSC_SCALE[1:0] and equation scaling.

Set CSC_SCALE high (2.58/2 = 1.29) and scale the overall equation by slightly more than 1.28 (coefficient falls within the supported range of [−0.999 … +0.999]).

CSC in Pass-Through Mode

It is possible to configure the CP CSC in a pass-through mode. In this mode, the CP CSC is used but does not alter the data it processes.

The CP CSC pass-through mode is obtained using the following settings:

1. Set MAN_CP_CSC_EN to 1'b1.
2. Set CSC_COEFF_SEL[3:0] to 4'b0000.
3. Leave the following registers from the CP map at the default:
   - CSC_SCALE = 1 (default value)
   - A4 = A3 = A2 = 0x000 (default value)
   - B4 = B3 = B1 = 0x000 (default value)
   - C4 = C2 = C1 = 0x000 (default value)
   - A1 = B2 = C3 = 0x800 (default value)

Note that the DPP CSC is always in pass-through mode unless the ADV7613 is processing an RGB input, outputting this input in the RGB color space and VID_ADJ_EN is enabled.

COLOR CONTROLS

The ADV7613 has a color control feature that can adjust the brightness, contrast, saturation, and hue properties.

VID_ADJ_EN, Address 44 (CP), Address 0x3E[7]

This bit is the video adjustment enable. This control selects whether or not the color controls feature is enabled. The color controls feature is configured via the CP_CONTRAST[7:0], CP_SATURATION[7:0], CP_BRIGHTNESS[7:0], and CP_HUE[7:0] parameters. The CP CSC must also be enabled for the color controls to be effective.

Table 239. VID_ADJ_EN Function Description

VID_ADJ_EN	Description
0 (default)	Disable color controls
1	Enable color controls

CP_CONTRAST[7:0], Address 44 (CP), Address 0x3A[7:0]

CP_CONTRAST[7:0] is a control to set the contrast. This field is a unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the contrast value, which is either 0 or 1. The seven LSBs represent the fractional part of the contrast value. The fractional part has the range [0 to 0.99]. This control is functional if VID_ADJ_EN is set to 1.

Table 240. CP_CONTRAST[7:0] Function Description

CP_CONTRAST[7:0]	Description
00000000	Contrast set to minimum
10000000 (default)	Default
11111111	Contrast set to maximum

CP_SATURATION[7:0], Address 44 (CP), Address 0x3B[7:0]

CP_SATURATION[7:0] is a control to set the saturation. This field is an unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the contrast value, which is either 0 or 1. The seven LSBs represent the fractional part of the saturation value. The fractional part has a [0 to 0.99] range. This control is functional if VID_ADJ_EN is set to 1.

Table 241. CP_SATURATION[7:0] Function Description

CP_SATURATION[7:0]	Description
00000000	Saturation set to minimum
10000000 (default)	Default
11111111	Saturation set to maximum

CP_BRIGHTNESS[7:0], Address 44 (CP), Address 0x3C[7:0]

CP_BRIGHTNESS[7:0] is a control to set the brightness. This field is a signed value. The effective brightness value applied to the luma is obtained by multiplying the programmed value CP_BRIGHTNESS with a gain of 4. The brightness applied to the luma has a range of [−512 to +508]. This control is functional if VID_ADJ_EN is set to 1.

Table 242. CP_BRIGHTNESS[7:0] Function Description

CP_BRIGHTNESS[7:0]	Description
00000000 (default)	The offset applied to the luma is 0.
01111111	The offset applied to the luma is 508d. This value corresponds to the brightness setting.
11111111	The offset applied to the luma is −512d. This value corresponds to the darkest setting.

CP_HUE[7:0], Address 44 (CP), Address 0x3D[7:0]

CP_HUE[7:0] is a control to set the hue. This register a represent an unsigned value which provides hue adjustment. Following control processes, Cb and Cr stream as follows:

$$Cb\_out = Cb \times \cos(hue) + Cr \times \sin(hue)$$

$$Cr\_out = Cr \times \cos(hue) - Cb \times \sin(hue)$$

It allows rotating of the hue by any angle <0; 360). This control is functional if VID_ADJ_EN is set to 1.

Table 243. CP_HUE[7:0] Function Description
Function

CP_HUE[7:0]	Description
0x00 (default)	A hue of 0° is applied to the chroma.
0x40	A hue of 90° is applied to the chroma.
0x80	A hue of 180° is applied to the chroma.
0xC0	A hue of 270° is applied to the chroma.

COMPONENT PROCESSOR

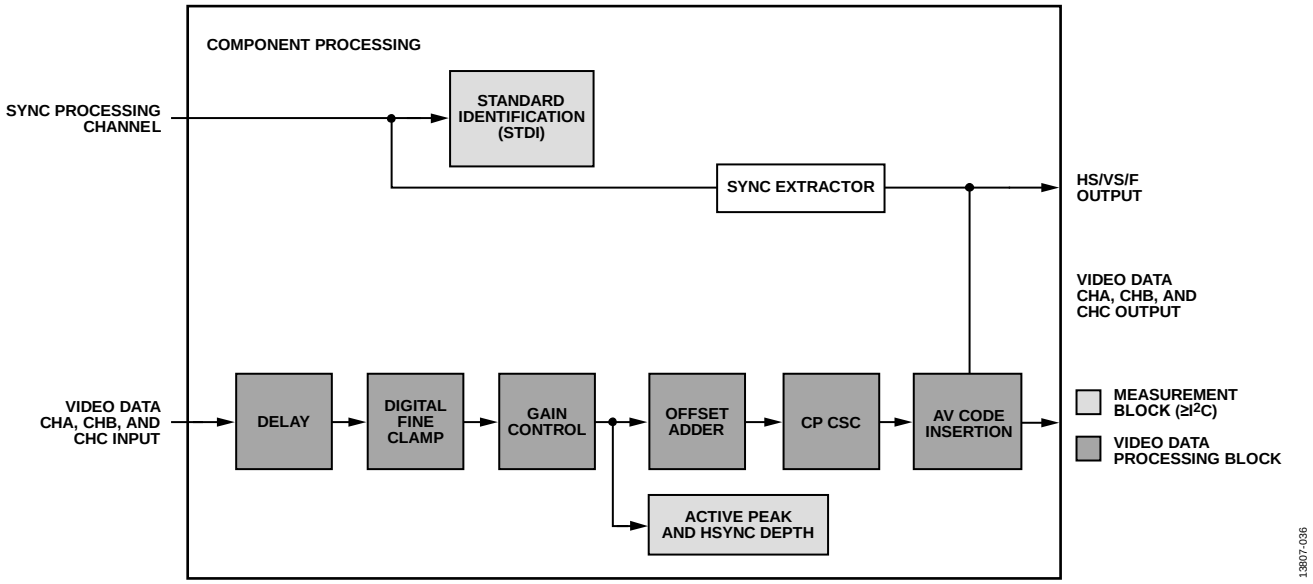


Figure 36. Component Processor Block Diagram

INTRODUCTION TO THE COMPONENT PROCESSOR

A simplified block diagram of the component processor (CP) on the ADV7613 is shown in Figure 36. Data is supplied to the CP from the data preprocessor (DPP). The CP circuitry is activated under the control of PRIM_MODE[3:0] and VID_STD[5:0].

The CP is designed to run at speeds of up to 170 MHz. Therefore, HDMI video with pixel clock frequencies above 170 MHz must be routed directly to the video output formatter, bypassing the data preprocessor (DPP) and component preprocessor (CP).

The CP is activated for the following modes of operation:

- Manual and automatic gain control
- Manual offset correction
- Saturation
- Insertion of timing codes and blanking data

The CP also has the following capabilities:

- Generates HSYNC, VSYNC, FIELD, and data enable (DE) timing reference outputs
- Color space conversion
- Color control adjustment

CLAMP OPERATION

The CP contains a digital fine clamp block. Its main purposes is to allow a clamp to operate even if the input signal is coming from a digital source.

The digital fine clamp operates in three separate feedback loops, one for each channel. The incoming video signal level is measured at the back porch. The level error, that is, clamp error, is compensated for by subtracting or adding a digital number to the data stream.

The digital clamp loop can be operated in an automatic or a manual mode with the following options:

- The clamp values for Channel B and Channel C can be set manually. This is the recommended mode.
- The clamp value is determined automatically on a line-by-line basis.
- The clamp loops can be frozen. This means that the currently active offsets are no longer updated but are applied permanently.
- The clamp value for Channel A can be set manually (static value).

Note that the target clamp level for black input is a digital code of 0, which facilitates the highest possible signal-to-noise ratio (SNR). Some interfaces (for example, ITU-R BT.656) require black to correspond to a value other than 0. To facilitate this requirement, there is an additional independent offset adder block after the gain multipliers for which separate fixed offset values can be supplied. See the CP Offset Block section for additional information.

CLMP_FREEZE, Address 44 (CP), Address 0x6C[5]

CLMP_FREEZE stops the digital fine clamp loops for Channel A, Channel B, and Channel C from updating.

Table 244. CLMP_FREEZE Function Description

CLMP_FREEZE	Description
0 (default)	Clamp value updated on every active video line
1	Clamp loops are stopped and not updated

CLMP_A_MAN, Address 44 (CP), Address 0x6C[7]

CLMP_A_MAN is the manual clamping enable for Channel A.

Table 245. CLMP_A_MAN Function Description

CLMP_A_MAN	Description
0 (default)	Ignore internal digital fine clamp loop result. Use CLMP_A[11:0].
1	Use the digital fine clamp value determined by the on-chip clamp loop.

CLMP_A[11:0], Address 44 (CP), Address 0x6C[3:0]; Address 0x6D[7:0]

CLMP_A[11:0] is the manual clamp value for Channel A. This field is an unsigned 12-bit value to be subtracted from the incoming video signal. This value programmed in this register is effective if the CLMP_A_MAN is set to 1. To change the CLMP_A[11:0], update Register Address 0x6C and Register Address 0x6D with the desired clamp value written to in this order and with no other I^2C access in between.

Table 246. CLMP_A[11:0] Function Description

CLMP_A[11:0]	Description
0x000 (default)	Minimum range
…	…
0xFFF	Maximum range

To facilitate an external clamp loop for Channel B and Channel C, the internal clamp value determined by the digital fine clamp block can be overridden by manual values programmed in the CP map. Both Channel B and Channel C are either in manual or automatic mode. There is no individual control for them.

The corresponding control values are CLMP_BC_MAN, CLMP_B[11:0], CLMP_C[11:0].

CLMP_BC_MAN, Address 44 (CP), Address 0x6C[6]

CLMP_BC_MAN is the manual clamping enable for Channel B and Channel C.

Table 247. CLMP_BC_MAN Function Description

CLMP_BC_MAN	Description
0 (default)	Ignore internal digital fine clamp loop result. Use CLMP_B[11:0] for Channel B and CLMP_C[11:0] for Channel C.
1	Use the digital fine clamp value determined by the on-chip clamp loop.

CLMP_B[11:0], Address 44 (CP), Address 0x6E[7:0]; Address 0x6F[7:4]

CLMP_B[11:0] is the manual clamp value for Channel B. This field is an unsigned 12-bit value to be subtracted from the incoming video signal. This value programmed in this register is effective if the CLMP_BC_MAN is set to 1. To change the CLMP_B[11:0], update Register Address 0x6E and Register Address 0x6F with the desired clamp value written to in this order and with no other I^2C access in between.

Table 248. CLMP_B[11:0] Function Description

CLMP_B[11:0]	Description
0x000 (default)	Minimum range
…	…
0xFFF	Maximum range

CLMP_C[11:0], Address 44 (CP), Address 0x6F[3:0]; Address 0x70[7:0]

CLMP_C[11:0] is the manual clamp value for Channel C. This field is an unsigned 12-bit value to be subtracted from the incoming video signal. This value programmed in this register is effective if the CLMP_BC_MAN is set to 1. To change the CLMP_C[11:0], update Register Address 0x6F and Register Address 0x70 with the desired clamp value written to in this order and with no other I²C access in between.

Table 249. CLMP_C[11:0] Function Description

CLMP_C[11:0]	Description
0x000 (default)	Minimum range
…	…
0xFFF	Maximum range

CP GAIN OPERATION

The digital gain block of the CP consists of three multipliers in the data paths of Channel A, Channel B, and Channel C, as well as one single automatic gain control loop. The gain control can be operated in manual or automatic mode.

Features of Manual Gain Control

The gain values for the three channels can be programmed separately via I²C registers. This is the recommended mode.

Features of Automatic Gain Control

The gain value is determined automatically, based on a signal with an embedded horizontal synchronization pulse on Channel A. The automatic gain control loop can be frozen, for example, after settling.

The gain value inputs are controlled via the OP_656_RANGE bit.

Manual Gain and Automatic Gain Control Selection

Figure 37 shows how the gain is applied to the video data processed by the CP section. The following gain configurations are available: automatic gain configuration in HDMI mode, and manual gain configuration.

Automatic gain configuration in HDMI mode is enabled by setting AGC_MODE_MAN to 0 and by setting the device in HDMI mode via PRIM_MODE[3:0] and VID_STD[5:0]. The gain applied to the video data depends on the input and output range configuration. The input range is set by control register INP_COLOR_SPACE and the readback register HDMI_COLORSPACE[3:0] as per Table 250. The output color space is determined the OP_656_RANGE control bit.

Manual gain configuration is enabled by setting AGC_MODE_MAN to 1 and GAIN_MAN to 1. The gain applied to the video data processed by the CP core is configured via the control registers A_GAIN[9:0], B_GAIN[9:0], and C_GAIN[9:0].

Table 250. Input Ranges for HDMI Modes

INP_COLOR_SPACE	Input Range
0b0000	16 to 235
0b0001	0 to 255
0b0010	16 to 235
0b0011	16 to 235
0b0100	0 to 255
0b0101	0 to 255
0b0110	0 to 255
0b0111	0 to 255
0b1111	16 to 235 if HDMI_COLORSPACE = 0b000 0 to 255 if HDMI_COLORSPACE = 0b001 16 to 235 if HDMI_COLORSPACE = 0b010 16 to 235 if HDMI_COLORSPACE = 0b011 0 to 255 if HDMI_COLORSPACE = 0b100 0 to 255 if HDMI_COLORSPACE = 0b101 0 to 255 if HDMI_COLORSPACE = 0b110 0 to 255 if HDMI_COLORSPACE = 0b111
0b1000 to 0b1110	Reserved

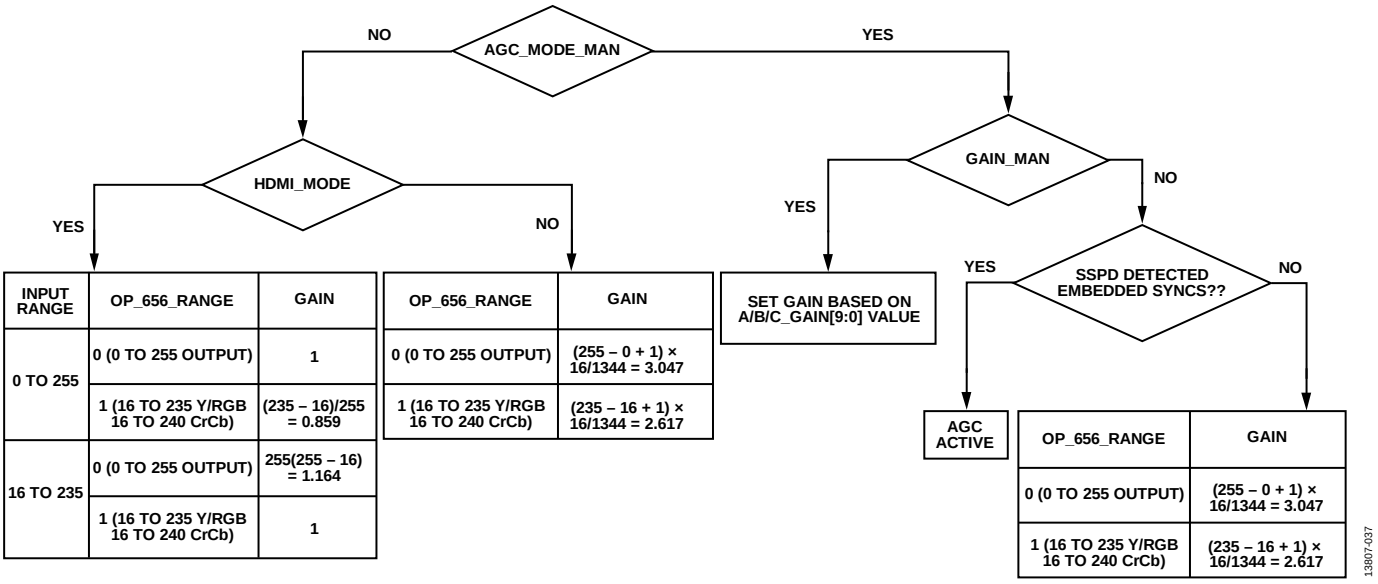


Figure 37. CP Automatic Gain Controls

AGC_MODE_MAN, Address 44 (CP), Address 0x73[6]

AGC_MODE_MAN is a control to set how the gains for all three channels are configured.

Table 251. AGC_MODE_MAN Function Description

AGC_MODE_MAN	Description
0 (default)	The gain is dependent on the type of input and OP_656_RANGE.
1	Gain operation controlled by GAIN_MAN.

Manual Gain Control

By setting the GAIN_MAN bit, the gain factors for Channel A, Channel B, and Channel C are no longer taken from the AGC, but are replaced by three dedicated I^2C registers.

Using these factors with the HSD_FB[11:0] register, it is possible to implement an off-chip AGC if desired. The range for the gain is [0…3.999]. The A_GAIN[9:0], B_GAIN[9:0], C_GAIN[9:0] registers are in 2.8 binary format and can be set as shown in Equation 8, CP manual gain.

$$X\_GAIN[9:0] = \text{floor}(GAIN \times 256) \quad (8)$$

where:
$0 \leq GAIN < 4$.
floor() is the floor function that returns the largest integer not greater than its input parameter.
X refers to A, B, and C.

Table 252. Example

Example Gain (Decimal)	A_GAIN[9:0]
0.5	0x80
0.98887	0xFD
2.5	0x280

GAIN_MAN, Address 44 (CP), Address 0x73[7]

GAIN_MAN enables the gain factor to be set by the AGC or manually.

Table 253. GAIN_MAN Function Description

GAIN_MAN	Description
0 (default)	AGC controls the gain for all three channels.
1	Manual gains are used for all three channels.

A_GAIN[9:0], Address 44 (CP), Address 0x73[5:0]; Address 0x74[7:4]

A_GAIN[9:0] is a control to set the manual gain value for Channel A.

This register is an unsigned value in a 2.8 binary format. To change A_GAIN[9:0], write to the register at Address 0x73 and Address 0x74 in this order with no I²C access in between.

Table 254. A_GAIN[9:0] Function Description

A_GAIN[9:0]	Description
0x000	Gain of 0
0x100 (default)	Unity gain
0x3FF	Gain of 3.99

B_GAIN[9:0], Address 44 (CP), Address 0x74[3:0]; Address 0x75[7:2]

B_GAIN[9:0] is a control to set the manual gain value for Channel B.

This register stores an unsigned value in a 2.8 binary format. To change B_GAIN[9:0], write to the register at Address 0x74 and Address 0x75 in this order with no I²C access in between.

Table 255. B_GAIN[9:0] Function Description

B_GAIN[9:0]	Description
0x000	Gain of 0
0x100 (default)	Unity gain
0x3FF	Gain of 3.99

C_GAIN[9:0], Address 44 (CP), Address 0x75[1:0]; Address 0x76[7:0]

C_GAIN[9:0] is a control to set the manual gain value for Channel C.

This register stores an unsigned value in a 2.8 binary format. To change C_GAIN[9:0], write to the register at Address 0x75 and Address 0x76 in this order with no I²C access in between.

Table 256. C_GAIN[9:0] Function Description

C_GAIN[9:0]	Description
0x000	Gain of 0
0x100 (default)	Unity gain
0x3FF	Gain of 3.99

HSD_FB[11:0], Address 44 (CP), Address 0xEB[3:0]; Address 0xEC[7:0] (Read Only)

HSD_FB[11:0] is a readback for the measured value of HSYNC depth on Channel A, after gain multiplier, for external feedback loop.

The value is presented in twos complement form, meaning that only a standard adder is needed to subtract the actual HSYNC depth (as per HSD_FB) from a nominal value, because the HSD_FB value is already in negative format.

Table 257. HSD_FB[11:0] Function Description

HSD_FB[11:0]	Description
xxxxxxxxxxxx	Readback value

Manual Gain Filter Mode

The ADV7613 provides a special filter option for the manual gain mode. This is functional only when manual gain is enabled. The purpose of this filter is a smoothing mechanism when the manual gain value is updated continuously by an external system based on either external or readback conditions in the ADV7613. The filter designed is an IIR filter with a transfer function of the form:

$$YN = (1 - A) \times YN - 1 + A \times XN$$

where A is the filter coefficient.

The values possible for A can vary from 1 (no filtering) to 1/128K (K = 1024). The value of coefficient A is chosen by programming CP_GAIN_FILT[3:0].

CP_GAIN_FILT[3:0], Address 44 (CP), Address 0x84[7:4]

A control to set the coefficient A of the IIF filter to filter the gain applied to the video signal when the gain is manually set. The value set in this register is effective only when manual gain is enabled. The filter is designed as an IIR filter with a transfer function of the form

$$Y[N] = (1 - A) \times y[N - 1] + A \times X[N]$$

Table 258. CP_GAIN_FILT[3:0] Function Description

CP_GAIN_FILT[3:0]	Description
0000 (default)	No filtering, that is, coefficient A = 1.
0001	Coefficient A = 1/128 lines.
0010	Coefficient A = 1/256 lines.
0011	Coefficient A = 1/512 lines.
0100	Coefficient A = 1/1024 lines.
0101	Coefficient A = 1/2048 lines.
0110	Coefficient A = 1/4096 lines.
0111	Coefficient A = 1/8192 lines.
1000	Coefficient A = 1/16,384 lines.
1001	Coefficient A = 1/32,768 lines.
1010	Coefficient A = 1/65,536 lines.
1011	Coefficient A = 1/131,072 lines.
All other values	Reserved. Do not use.

Other Gain Controls

OP_656_RANGE, IO, Address 0x02[2]

This bit is a control to set the output range of the digital data. It also automatically the data saturator setting.

Table 259. OP_656_RANGE Function Description

OP_656_RANGE	Description
0 (default)	Enables full output range (0 to 255)
1	Enables limited output range (16 to 235)

Table 260. OP_656_RANGE Description for HDMI Receiver Input Mode

Input Range	OP_656_RANGE	Gain
0 to 255	0 (0 to 255 output)	1
	1 (16 to 235 RGB output, 16 to 240 CrCb output)	(235 − 16)/255 = 0.859
16 to 235	0 (0 to 255 output)	255/(235 − 16) = 1.164
	1 (16 to 235 RGB output, 16 to 240 CrCb output)	1

Table 261. OP_656_RANGE Description for Analog Front-End Input Mode

OP_656_RANGE	Gain
0 (0 to 255 output)	(255 − 0 + 1) × 16/1792 = 2.29
1 (16 to 235 RGB output, 16 to 240 CrCb output)	(235 − 16 + 1) × 16/1792 = 1.96

ALT_DATA_SAT, IO, Address 0x02[0]

This bit is a control to disable the data saturator that limits the output range independently of OP_656_RANGE. This bit is used to support extended data range modes.

Table 262. ALT_DATA_SAT Function Description

ALT_DATA_SAT	Description
0 (default)	Data saturator enabled or disabled according to OP_656_RANGE setting
1	Reverses OP_656_RANGE decision to enable or disable the data saturator

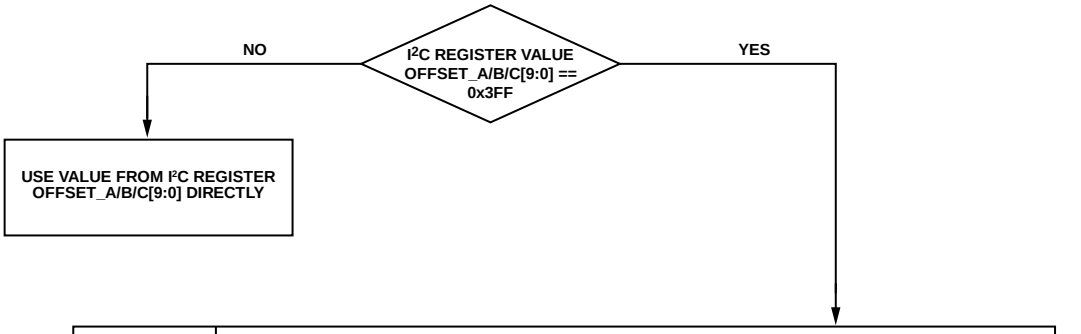
CP OFFSET BLOCK

The offset block consists of three independent adders, one for each channel. Using the A_OFFSET, B_OFFSET, and C_OFFSET registers, a fixed offset value can be added to the data. The actual offset used can come from two different sources:

The ADV7613 includes an automatic selection of the offset value, dependent on the CSC mode that is programmed by the user. The RGB_OUT and OP_656_RANGE bits are used to derive offset values.

A manual, user defined value can be programmed.

When the offset registers (A_OFFSET, B_OFFSET, and C_OFFSET) contain the value 0x3FF (reset default), the offset used is determined using the automatic selection process. For any other value in the offset registers, the automatic selection is disabled and the user-programmed offset value is applied directly to the video. Refer to the flowchart in Figure 38.



CHANNEL	OFFSET			
	RGB_OUT = 1		RGB_OUT = 0	
	OP_656_RANGE = 1	OP_656_RANGE = 0	OP_656_RANGE = 1	OP_656_RANGE = 0
A	64dec	0dec	64dec	0dec
B	64dec	0dec	512dec	512dec
C	64dec	0dec	512dec	512dec

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Figure 38. Channel A, Channel B, and Channel C Automatic Value Selection

For RGB type output data, the three offset values must be programmed to 0 or 64 (desired code output for black video). For YPbPr type output data, A_OFFSET[9:0] must be set to 64 (desired code for black); B_OFFSET[9:0] and C_OFFSET[9:0] (for Pr and Pb) are typically set to 512 (midrange).

Note that adding an excessive offset onto the data results in clipping of the signal. The offset value can only be positive; it is an unsigned number. The ADV7613 employs sequencers for the offset values that prohibit intermediate wrong values to be applied.

The I²C sequencer treats the three offset values as separate entities. To update all three offset values, a single sweep of I²C writes to the CP map, Register 0x77, Register 0x78, Register 0x79, and Register 0x7A is sufficient.

A_OFFSET[9:0], Address 44 (CP), Address 0x77[5:0]; Address 0x78[7:4]

A_OFFSET[9:0] is a control to set the manual offset for Channel A.

This field stores an unsigned value. To change A_OFFSET[9:0], Register Address 0x77 and Register Address 0x78 must be written to in this order with no I²C access in between.

Table 263. A_OFFSET[9:0] Function Description

A_OFFSET[9:0]	Description
0x3FF (default)	Automatic offset to Channel A
Any other value	Channel A offset

Note that to change the A_OFFSET[9:0] value, Register 0x77 and Register 0x78 must be written to in this order with no other I²C access in between.

B_OFFSET[9:0], Address 44 (CP), Address 0x78[3:0]; Address 0x79[7:2]

B_OFFSET[9:0] is a control to set the manual offset for Channel B.

This field stores an unsigned value. To change B_OFFSET[9:0], Register Addresses 0x78 and Register Address 0x79 must be written to in this order with no I²C access in between.

Table 264. B_OFFSET[9:0] Function Description

B_OFFSET[9:0]	Description
0x3FF (default)	Automatic offset to Channel B
Any other value	Channel B offset

Note that to change the A_OFFSET[9:0] value, Register 0x77 and Register 0x78 must be written to in this order with no other I²C access in between.

C_OFFSET[9:0], Address 44 (CP), Address 0x79[1:0]; Address 0x7A[7:0]

C_OFFSET[9:0] is a control to set the manual offset for Channel C.

This field stores an unsigned value. To change C_OFFSET[9:0], Register Address 0x79 and Register Address 0x7A must be written to in this order with no I²C access in between.

Table 265. C_OFFSET[9:0] Function Description

C_OFFSET[9:0]	Description
0x3FF (default)	Automatic offset to Channel C
Any other value	Channel C offset

Note that to change the A_OFFSET[9:0] value, Register 0x77 and Register 0x78 must be written to in this order with no other I²C access in between.

CP DATA PATH FOR HDMI MODES

Figure 39 and Figure 40 depict the data path of the video for HDMI mode. These figures depict the gains and offsets applied when using the automatic control, OP_656_RANGE, and the manual options for setting the clamp level, gain, and offset.

The I²C settings are detailed in Table 266 for use when processing extended range video signals with blacker than black and/or whiter than white video levels.

Table 266. Settings Required to Support Extended Range Video Input

I²C Setting/Mode	Analog Modes	HDMI Mode YUV	HDMI Mode RGB [0 to 255]	HDMI Mode RGB [16 to 235]
OP_656_RANGE	1	1	0	1
ALT_DATA_SAT	1	1	0	1

Pregain Block

To compensate for signal attenuation in the analog front end of the ADV7613 and input buffer gain, a pregain block is provided in the CP path. The pregain block is controlled by CP_MODE_GAIN_ADJ[7:0], which represents an unsigned value in a 1.7 binary format. The range of CP_MODE_GAIN_ADJ[7:0] is 0 to 1.99.

The MSB of CP_MODE_GAIN_ADJ[7:0] represents the integer part of the pregain value while the 7 LSBs represents the fractional part of the pregain value.

CP_MODE_GAIN_ADJ[7:0], Address 44 (CP), Address 0x40[7:0]

CP_MODE_GAIN_ADJ[7:0] is the pregain adjustment to compensate for the gain of the analog front end. This register stores a value in a 1.7 binary format.

Table 267. CP_MODE_GAIN_ADJ[7:0] Function Description

CP_MODE_GAIN_ADJ[7:0]	Description
0xxxxxxx	Gain of (0 + (xxxxxxx/128))
10000000	Default pregain (pregain of 1.0)
1xxxxxxx	Gain of (1 + (xxxxxxx/128))

CP_MODE_GAIN_ADJ_EN, Address 44 (CP), Address 0x3E[2]

CP_MODE_GAIN_ADJ_EN is a control to enable pregain.

Table 268. CP_MODE_GAIN_ADJ_EN Function Description

CP_MODE_GAIN_ADJ_EN	Description
0 (default)	The pregain block is bypassed.
1	The pregain block is enabled.

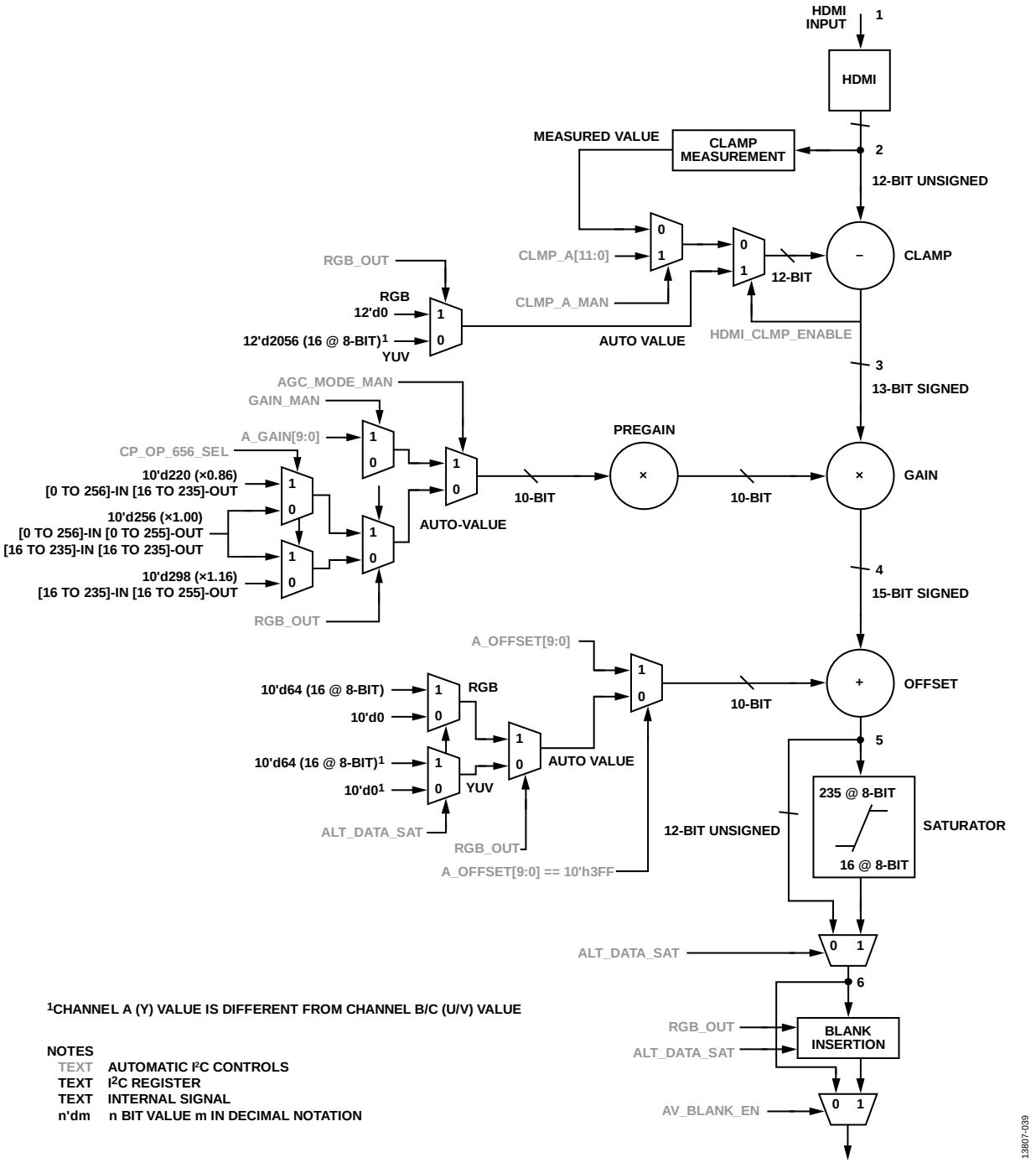

Figure 39. CP Data Path Channel A (Y) for HDMI Mode

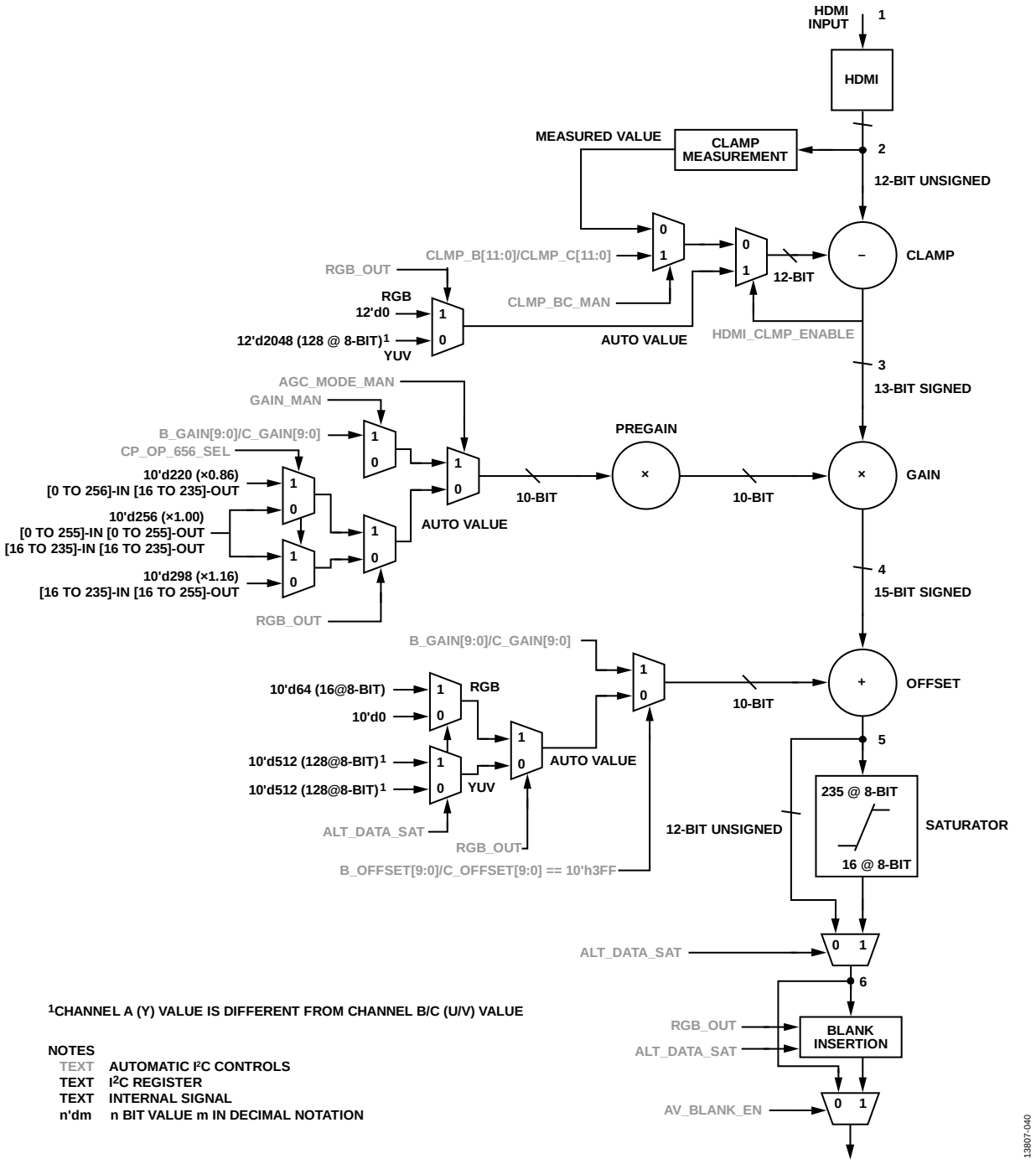

Figure 40. CP Data Paths Channel B and Channel C for HDMI Mode

SYNC PROCESSED BY CP SECTION

The CP core uses the HDMI section as its source of HSYNC, VSYNC and DE.

Sync Routing from HDMI Section

The CP section receives syncs from the HDMI section, as shown in Figure 41.

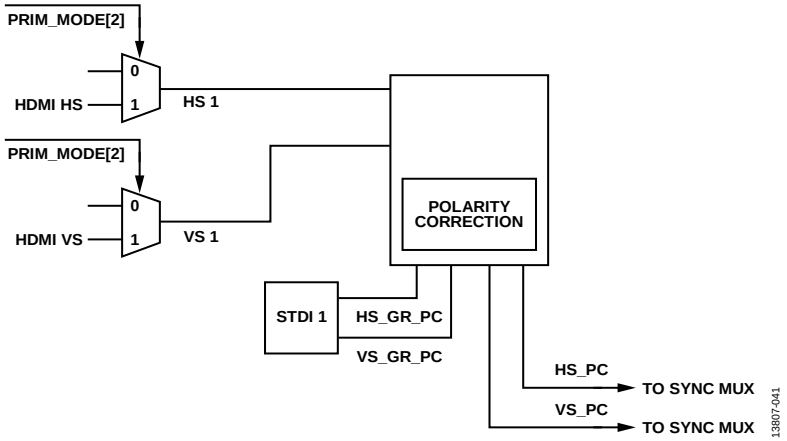

Figure 41. External/HDMI Syncs Routing to CP Section

Signals Routing to Synchronization Channels

The ADV7613 has one synchronization channel consisting of one STDI section. When an HDMI input is applied, the HDMI core generates HSYNC, VSYNC, and DE signals and supply them as input to the each synchronization channel shown in Figure 41. HSYNC from the HDMI block is denoted as HDMI_HS, and VSYNC from the HDMI block is denoted as HDMI_VS. DE from the HDMI block is not shown in Figure 41 as it is passed directly to the CP core without any processing when an HDMI input is selected.

Standard Detection and Identification

As shown in Figure 41, the synchronization channel also contains standard detection and identification (STDI) block. These monitor the synchronization signals to determine the video input standard.

The STDI blocks perform four key measurements:

- Block length CH1_BL[13:0]: this is the number of 28.6363 MHz clock cycles (XTAL frequency) in a block of eight lines. From this number, the time duration of one line can be concluded.
- Line count in Field CH1_LCF[10:0]: the CH1_LCF[10:0] readback value is the number of lines between two VSYNCs, that is, over one field measured by channel.
- Line count in VSYNC CH1_LCVS[4:0]: the LCVS[4:0] readback value is the number of lines within one VSYNC period.
- Field length CH1_FCL[12:0]: this is the number of 28.6363 MHz clock cycles in a 1/256th of a field. Alternately, this value of FCL multiplied by 256 gives one field length count in 28.6363 MHz (XTAL) clocks.

By interpreting these four parameters, it is possible to distinguish between the different types of input signals.

In ADV7613, there are three operational modes for the STDI block:

- Continuous mode: the STDI block performs continuous measurements on lock/unlock bases and updates the corresponding I^{2}C registers based on the lock status bit (STDI_DVALID).
- Real-time continuous mode: the STDI block performs continuous measurement regardless of the lock/unlock bases and always updates real-time measurement data to the corresponding I^{2}C registers.
- Single-shot mode: the STDI block waits for a trigger (0 to 1 transition on CH1_TRIG_STDI) to start the measurements. Single-shot mode can be useful in complex systems where the scheduling of functions is important.

A data valid flag, CH1_STDI_DVALID, is provided, which is based on the status of the horizontal/vertical lock of the block and is held low during the measurements. The four parameters must only be read after the CH1_STDI_DVALID flag has gone high for the continuous/single-shot mode. In real-time continuous mode, the ADV7613 allows the user to monitor the real-time timing measurement regardless of the CH1_STDI_DVALID flag. Refer to the STDI Readback Values section for information on the readback values.

Note that synchronization type pulses include horizontal synchronization, equalization and serration pulses.

The CH1_TRIG_STDI flag is not self clearing. The measurements are only started upon setting the CH1_TRIG_STDI flag, which means that after setting it, it must be cleared again by writing a 0 to it. This second write (to clear the flag) can be done at any time and does not have any effect on running measurements. It also does not invalidate previous measurement results.

The ADV7613 only measures those parameters, but does not take any action based upon them. The device does not reconfigure itself. To avoid unforeseen problems in the scheduling of a system controller, the device only helps to identify the input.

Because real-time continuous mode provides the capability to monitor the real-time measurement data regardless of the block lock status, the user must be aware that the timing readback values may not be a valid readback measurement in this mode.

CH1_STDI_CONT, Address 44 (CP), Address 0x86[1]

This bit is a control to set the synchronization source polarity detection mode for Sync Channel 1 STDI.

Table 269. CH1_STDI_CONT Function Description

CH1_STDI_CONT	Description
0	Sync Channel 1 STDI works in one-shot mode (triggered by a 0 to 1 transition on the CH1_TRIG_STDI bit)
1 (default)	Sync Channel 1 STDI works in continuous mode

BYPASS_STDI1_LOCKING, Address 44 (CP), Address 0xF5[1]

This bit bypasses STDI locking for Sync Channel 1.

Table 270. BYPASS_STDI1_LOCKING Function Description

BYPASS_STDI1_LOCKING	Description
0 (default)	Update CH1_BL, CH1_LCF, and CH1_LCVS after the sync Channel 1 STDI locks and CH1_STDI_DVALID is set to 1.
1	Update CH1_BL, CH1_LCF,CH1_LCVS from the sync Channel 1 STDI as they are measured.

CH1_TRIG_STDI, Address 44 (CP), Address 0x86[2]

This bit is the trigger synchronization source and polarity detector for Sync Channel 1 STDI. A 0-to-1 transition in this bit restarts the autosync detection algorithm. This is not a self clearing bit and must be set to 0 to prepare for the next trigger.

Table 271. CH1_TRIG_STDI Function Description

CH1_TRIG_STDI	Description
0 (default)	Default value—transition 0 to 1 restarts auto-sync detection algorithm
1	Transition 0 to 1 restarts auto-sync detection algorithm

CH1_STDI_DVALID, Address 44 (CP), Address 0xB1[7] (Read Only)

This bit is set when the measurements performed by Sync Channel 1 STDI are completed. High level signals validity for CH1_BL, CH1_LCF, CH1_LCVS, CH1_FCL, and CH1_STDI_INTLCD parameters. To prevent false readouts, especially during signal acquisition, CH1_SDTI_DVALID only goes high after four fields with same length are recorded. As a result, STDI measurements can take up to five fields to finish.

Table 272. CH1_STDI_DVALID Function Description

CH1_STDI_DVALID	Description
0 (default)	Sync Channel 1 STDI measurements are not valid.
1	Sync Channel 1 STDI measurements are valid.

CP_STDI_INTERLACED, IO, Address 0x12[4] (Read Only)

This bit is a readback to indicate the interlaced status of the currently selected STDI block applied to the CP core.

Table 273. CP_STDI_INTERLACED Function Description

CP_STDI_INTERLACED	Description
0 (default)	Selected STDI has detected a progressive input.
1	Selected STDI has detected a interlaced input.

CP_INTERLACED, IO, Address 0x12[3] (Read Only)

This bit is a readback to indicate the interlaced status of the CP core based on configuration of video standard and INTERLACED bit in the CP map.

Table 274. CP_INTERLACED Function Description

CP_INTERLACED	Description
0 (default)	CP core is processing the input as a progressive input.
1	CP core is processing the input as a interlaced input.

CP_PROG_PARM_FOR_INT, IO, Address 0x12[2] (Read Only)

This bit is a readback to indicate if the CP core is processing for progressive standard while the vdeo standard and the INTERLACED bit in the CP map are configured for an interlaced standard.

Table 275. CP_PROG_PARM_FOR_INT Function Description

CP_PROG_PARM_FOR_INT	Description
0 (default)	CP core processing for a progressive standard while video standard and the INTERLACED bits are configured for an interlaced standard
1	CP core processing for a progressive standard while video standard and the INTERLACED bits are configured for a progressive standard

CP_FORCE_INTERLACED, IO, Address 0x12[1] (Read Only)

This bit is a readback to indicate forced-interlaced status of the CP core based on configuration of video standard and INTERLACED bit in the CP map.

Table 276. CP_FORCE_INTERLACED Function Description

CP_FORCE_INTERLACED	Description
0 (default)	Input is detected as interlaced and the CP is programmed in an interlaced mode via VID_STD[5:0].
1	Input is detected as progressive and the CP is programmed in an interlaced mode.

Detailed Mechanism of STDI Block Horizontal/Vertical Lock Mechanism

STDI Horizontal Locking Operation

For the STDI horizontal locking operation, the STDI block compares adjacent line length differences (in XTAL clock cycles) with the programmed threshold. If 128 consecutive adjacent lines lengths are within the threshold, the STDI horizontally locks to the incoming video.

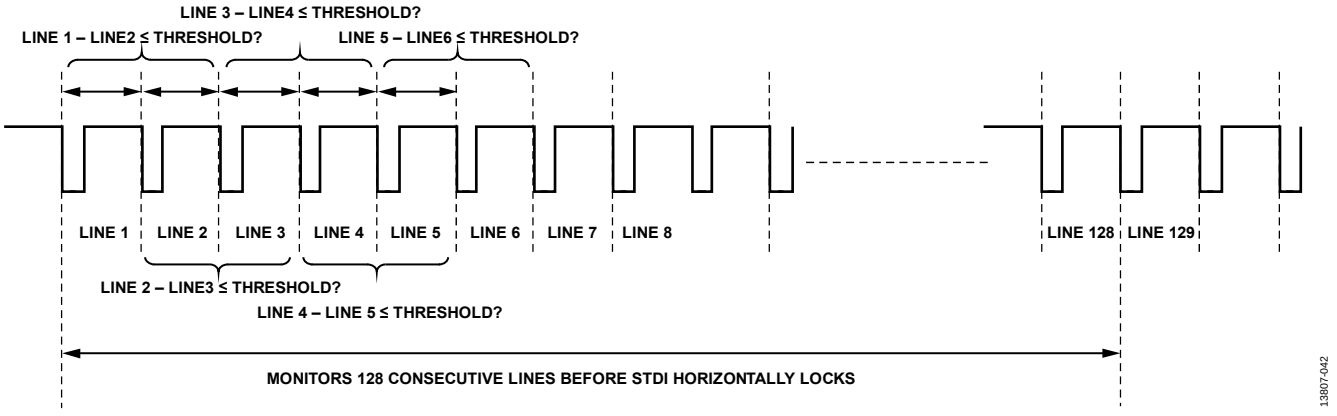

Figure 42. STDI Horizontal Locking Operation

Once the STDI locks to the incoming video, it registers the first BL measurement (first eight lines) as latched data (absolute line length: L) and keeps monitoring and comparing each successive line length with the absolute line length (L/8).

The STDI horizontally unlocks if 128 consecutive lines have a line length greater than the threshold.

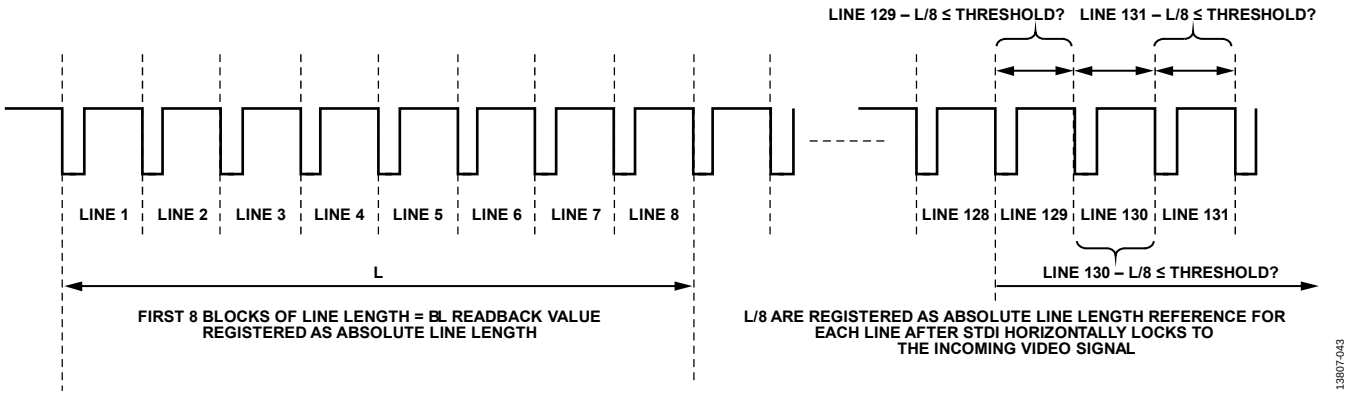

Figure 43. STDI HSYNC Monitoring Operation

STDI Vertical Locking

The STDI block compares adjacent field length differences and VSYNC lengths in line counts and compares them with a threshold. If four consecutive adjacent field lengths (LCF) and line counts in VSYNC (LCVS) are within the threshold, the STDI locks vertically to the incoming video.

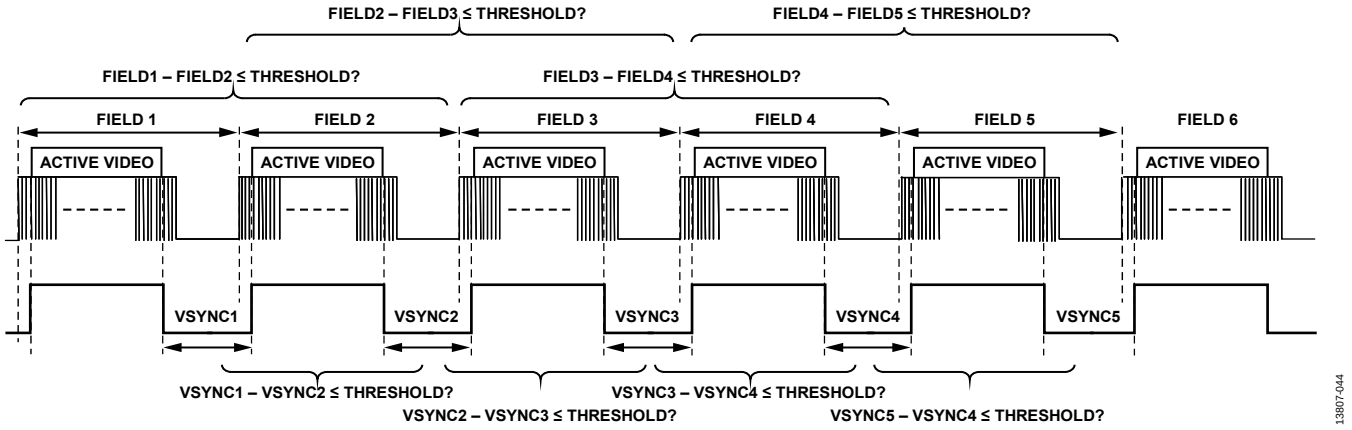

Figure 44. STDI Vertical Locking Operation

Once the STDI locks to the incoming video, the STDI registers the latest field length/VSYNC length as latched data (absolute field length: F, absolute VSYNC length: V). The STDI keeps monitoring and comparing FIELD/VSYNC lengths with the respective absolute length (F, V) once vertically locked. The STDI vertically unlocks if four consecutive FIELD or VSYNC lengths are greater than the respective threshold.

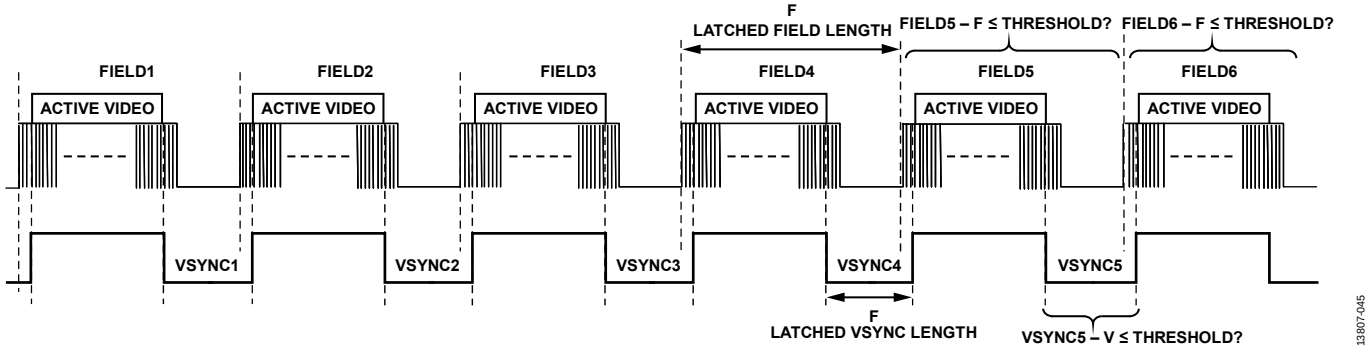

Figure 45. STDI VSYNC Monitoring Operation

CH1_BL[13:0], Address 44 (CP), Address 0xB1[5:0]; Address 0xB2[7:0] (Read Only)

CH1_BL[13:0] is a readback for the block length for Sync Channel 1. Number of crystal cycle cycles in a block of eight lines of incoming video. This readback is valid if CH1_STDI_DVALID is high.

Table 277. CH1_BL[13:0] Function Description

CH1_BL[13:0]	Description
xxxxxxxxxxxxxx	Readback value

CH1_LCVS[4:0], Address 44 (CP), Address 0xB3[7:3] (Read Only)

CH1_LCVS[4:0] is a readback for the Sync Channel 1 line count in a VSYNC, the number of lines in a VSYNC period measured on Sync Channel 1. The readback from this field is valid if CH1_STDI_DVALID is high.

Table 278. CH1_LCVS[4:0] Function Description

CH1_LCVS[4:0]	Description
xxxxx	Readback value

CH1_LCF[11:0], Address 44 (CP), Address 0xA3[3:0]; Address 0xA4[7:0] (Read Only)

CH1_LCF[11:0] is a readback for the Sync Channel 1 line count in a field, the number of lines between two VSYNCs measured on Sync Channel 1. The readback from this field is valid if CH1_STDI_DVALID is high.

Table 279. CH1_LCF[11:0] Function Description

CH1_LCF[11:0]	Description
xxxxxxxxxxx	Readback value

CH1_FCL[12:0], Address 44 (CP), Address 0xB8[4:0]; Address 0xB9[7:0] (Read Only)

CH1_FCL[12:0] is a readback for the Sync Channel 1 field count length, the number of crystal clock cycles between successive VSYNCs measured by Sync Channel 1 STDI or in 1/256th of a field. The readback from this field is valid if CH1_STDI_DVALID is high.

Table 280. CH1_FCL[12:0] Function Description

CH1_FCL[12:0]	Description
xxxxxxxxxxxxx	Readback value

CH1_STDI_INTLCD, Address 44 (CP), Address 0xB1[6] (Read Only)

This bit is the interlaced vs. progressive mode detected by Sync Channel 1 STDI. The readback from this register is valid if CH1_STDI_DVALID is high.

Table 281. CH1_STDI_INTLCD Function Description

CH1_STDI_INTLCD	Description
0 (default)	Indicates a video signal on Sync Channel 1 with noninterlaced timing
1	Indicates a signal on Sync Channel 1 with interlaced timing

STDI Usage

Figure 46 shows a flowchart of the intended usage of the STDI block.

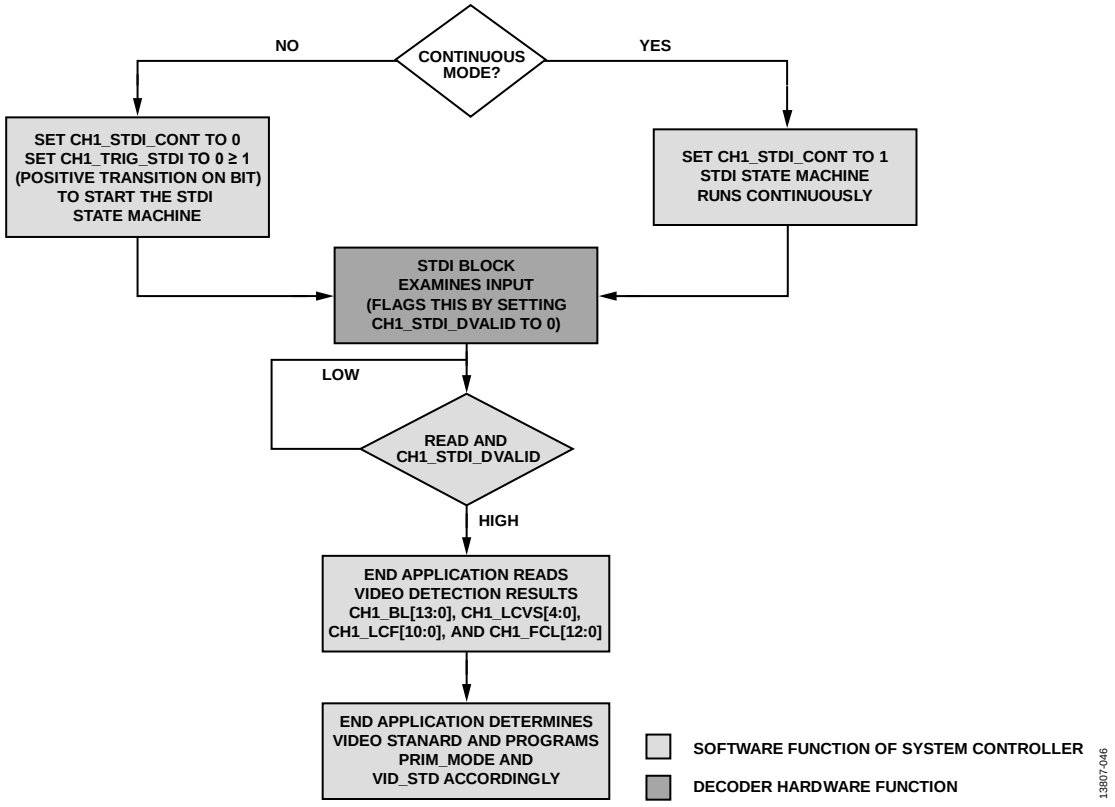

Figure 46. STDI Usage Flowchart

STDI Readback Values

Table 282. STDI Readback Values for SD, PR, and HD

Standard[1]	CHx_BL[13:0], 28.63636 MHz XTAL	CHx_LCF[10:0]	CHx_LCVS[4:0]	FCL[12:0], 28.63636 MHz XTAL
720p SMPTE 296M	5091	750	4 to 5	1868
525p BT 1358	7270	525	5 to 6	1868
625p BT 1358	7331	625	4 to 5	2237
1125p SMPTE 274M 10	848	1125	4 to 5	1868

[1] SMPTE stands for the Society of Motion Picture and Television Engineers.

The values of LCF and LCVS do not change with the XTAL frequency.

STDI Readback Values for GR

Table 283. STDI Results for Graphics Standards

Standard	CHx_BL[13:0] 28.63636 MHz XTAL	CHx_LCF[10:0]	CHx_LCVS[4:0]	FCL[12:0] 28.63636 MHz XTAL
XGA 85	3327	805 to 808	0 to 3	1316
SXGA 60	3571	1063 to 1066	0 to 3	1868
XGA 75	3808	797 to 800	0 to 3	1493
XGA 70	4048	800 to 806	0 to 6	1598
SVGA 85	4259	628 to 631	0 to 3	1316
XGA 60	4726	800 to 806	0 to 6	1868
SVGA 72	4756	660 to 666	0 to 6	1554
SVGA 75	4878	622 to 625	0 to 3	1493
VGA 85	5286	506 to 509	0 to 3	1316
VGA 72	6042	517 to 520	0 to 3	1554
SVGA 60	6039	624 to 628	0 to 4	1868
VGA 75	6098	497 to 500	0 to 3	1493
SVGA 56	6508	623 to 625	0 to 2	1997
VGA 60	7272	523 to 525	0 to 2	1868

Figure 47 shows the parameters from Table 283 plotted against each other at the recommended 28.63636 MHz XTAL operation.

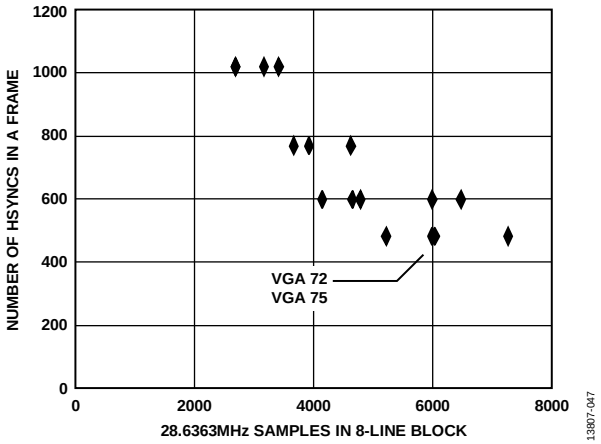

Figure 47. STDI Values for GR Mode

Note that although the two points for VGA72 and VGA75 look very close, it is anticipated that the difference in the parameters is sufficient to distinguish between them.

HDMI_CP_LOCK_THRESHOLD[1:0], Address 44 (CP), Address 0xCB[1:0]

HDMI_CP_LOCK_THRESHOLD[1:0] is the locking time of the filter used for buffering of timing parameters in HDMI mode.

Table 284. HDMI_CP_LOCK_THRESHOLD[1:0] Function Description

HDMI_CP_LOCK_THRESHOLD[1:0]	Description
00 (default)	Slowest locking time
01	Medium locking time
10	Fastest locking time
11	Fixed step size of 0.5 pixels

FREE RUN MODE

Free run mode provides the user with a stable clock and predictable data if the input signal cannot be decoded, for example, if input video is not present. It controls default color insertion and causes the ADV7613 to generate a default clock. The state in which this happens can be monitored via the CP_FREE_RUN status bit (see the CP Status section for more information.). The free run feature is not configured automatically for HDMI modes. In addition, the ADV7613 can free run only to HDMI video up to 2.25 Gbps.

Free Run Mode Thresholds

The free run threshold parameters define the horizontal and vertical conditions under which free run mode is entered. The horizontal and vertical parameters of the incoming video signal are measured and compared with internally stored parameters, and the magnitude of the difference decides whether to enter free run. The internally stored parameters are decoded by default from PRIM_MODE[3:0] and VID_STD[5:0]. For video standards other than the preprogrammed settings of PRIM_MODE[3:0] and VID_STD[5:0], the parameters can be set manually.

Horizontal Conditions

In the case of the horizontal conditions, the length of the incoming video line is measured based on the 28.6363 MHz crystal clock. This value is compared with the internally stored horizontal parameter, the ideal line length. The CH1_F_RUN_TH[2:0] control bits allow the user to select the threshold for Channel 1. The ideal line length can be manually set via the free run line length control, CH1_FR_LL[10:0].

CH1_F_RUN_THR[2:0], Address 44 (CP), Address 0xF3[2:0]

CH1_F_RUN_THR[2:0] is the free run threshold select for Sync Channel 1. It determines the horizontal conditions under which free run mode is entered or left. The length of the incoming video line is measured based on the crystal clock and compared to an internally stored parameter. The magnitude of the difference decides whether or not Sync Channel 1 enters free run mode.

Table 285. CH1_F_RUN_THR[2:0] Function Description

CH1_F_RUN_THR[2:0]	Description
000	Minimum difference to switch into free run is 2. Maximum difference to switch out of free run is 1.
001	Minimum difference to switch into free run is 256. Maximum difference to switch out of free run is 200.
010	Minimum difference to switch into free run is 128. Maximum difference to switch out of free run is 112.
011	Minimum difference to switch into free run is 64. Maximum difference to switch out of free run is 48.
100 (default)	Minimum difference to switch into free run is 32. Maximum difference to switch out of free run is 24.
101	Minimum difference to switch into free run is 16. Maximum difference to switch out of free run is 12.
110	Minimum difference to switch into free run is 8. Maximum difference to switch out of free run is 6.
111	Minimum difference to switch into free run is 4. Maximum difference to switch out of free run is 3.

CH1_FR_LL[10:0], Address 44 (CP), Address 0x8F[2:0]; Address 0x90[7:0]

CH1_FR_LL[10:0] is the free run line length in number of crystal clock cycles in one line of video for Sync Channel 1 STDI. This register must only be programmed using video standards that are not supported by PRIM_MODE[3:0] and VID_STD[5:0].

Table 286. CH1_FR_LL[10:0] Function Description

CH1_FR_LL[10:0]	Description
0x000 (default)	Internal free run line length is decoded from PRIM_MODE[3:0] and VID_STD[5:0].
All other values	Number of crystal clocks in the ideal line length. Used to enter or exit free run mode.

Note that this parameter has no effect on the video decoding. If CH1_FR_LL[10:0] is not programmed, the free run line length parameter is decoded from PRIM_MODE[3:0] and VID_STD[5:0].

Vertical Conditions

In the case of the vertical conditions, the STDI section measures the number of lines per field of incoming video signal. This value is compared with an internally stored vertical parameter, the ideal field length. The CH1_FL_FR_THRESHOLD[1:0] control bits allow the user to select the threshold for Channel 1. The ideal number of lines per field can be set manually via the CP_LCOUNT_MAX[11:0] register.

CH1_FL_FR_THRESHOLD[2:0], Address 44 (CP), Address 0xF3[5:3]

CH1_FL_FR_THRESHOLD[2:0] is the threshold for difference between input video field length and internally stored standard to enter and exit free run.

Table 287. CH1_FL_FR_THRESHOLD[2:0] Function Description

CH1_FL_FR_THRESHOLD[2:0]	Description
000	Minimum difference to switch into free run is 36 lines. Maximum difference to switch out of free run is 31 lines.
001	Minimum difference to switch into free run is 18 lines. Maximum difference to switch out of free run is 15 lines.
010 (default)	Minimum difference to switch into free run is 10 lines. Maximum difference to switch out of free run is 7 lines.
011	Minimum difference to switch into free run is 4 lines. Maximum difference to switch out of free run is 3 lines.
100	Minimum difference to switch into free run is 51 lines. Maximum difference to switch out of free run is 46 lines.
101	Minimum difference to switch into free run is 69 lines. Maximum difference to switch out of free run is 63 lines.
110	Minimum difference to switch into free run is 134 lines. Maximum difference to switch out of free run is 127 lines.
111	Minimum difference to switch into free run is 263 lines. Maximum difference to switch out of free run is 255 lines.

CP_LCOUNT_MAX[11:0], Address 44 (CP), Address 0xAB[7:0]; Address 0xAC[7:4]

CP_LCOUNT_MAX[11:0] is the manual value for total number of lines in a frame expected by the CP core. CP_LCOUNT_MAX[11:0] is an unsigned value. This register is used for manual configuration of the free run feature. The value programmed in this register is used for Sync Channel 1. The value programmed in this register is used also for Sync Channel 2 if CH2_FR_FIELD_LENGTH[10:0] is set to 0x000.

Table 288. CP_LCOUNT_MAX[11:0] Function Description

CP_LCOUNT_MAX[11:0]	Description
0x000 (default)	Ideal number of lines per frame is decoded from PRIM_MODE[3:0] and VID_STD[5:0] for Sync Channel 1.
All other values	Use the programmed value as ideal number of lines per frame in free run decision for Sync Channel 1.

INTERLACED, Address 44 (CP), Address 0x91[6]

INTERLACED sets the interlaced/progressive mode of the incoming video processed in CP mode.

Table 289. INTERLACED Function Description

INTERLACED	Description
0	The CP core expects progressive video mode
1 (default)	the CP core expects interlaced video mode

Field line count is the vertical parameter that holds the ideal number of lines per field for a given video standard. It affects the way CP handles the unlocked state. It affects the way CP handles the unlocked state. If CP_LCOUNT_MAX[11:0] is set to 0, the internally used free run line length value is decoded from the current setting of PRIM_MODE[3:0] and VID_STD[5:0].

For standards not covered by the preprogrammed values, the CP_LCOUNT_MAX[11:0] and INTERLACED parameters must be set to the ideally expected number of lines per field.

Note that the CP_LCOUNT_MAX[11:0] parameter has no effect on the video decoding. If CP_LCOUNT_MAX[11:0] is not programmed, the free run line length parameter is decoded from PRIM_MODE[3:0] and VID_STD[5:0]. If CP_LCOUNT_MAX[11:0] is programmed, then free run line length parameter defined by CP_LCOUNT_MAX[11:0] and INTERLACED, is used for Channel 1.

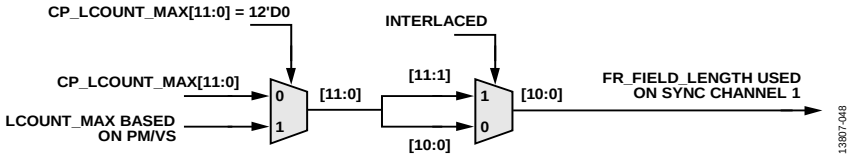

Figure 48. Free Run Field Length Selection for Channel 1 and Channel 2

Free Run Feature in HDMI Mode

This section describes how to configure the free run feature when the ADV7613 is in HDMI mode. The ADV7613 HDMI mode is defined in the Primary Mode and Video Standard section.

There are two free run modes in HDMI: Free Run Mode 0 and Free Run Mode 1. The HDMI_FRUN_MODE control selects which free run mode is enabled.

- HDMI Free Run Mode 0: the decoder enters free run when the TMDS clock is not detected, for example, in a cable disconnect situation.
- HDMI Free Run Mode 1: the decoder enters free run when the TMDS clock is not detected or when the detected input format does not match the format dictated by the PRIM_MODE[3:0] and VID_STD[5:0] settings.

For either free run mode to be implemented, HDMI free run operation must be enabled. This is done via the HDMI_FRUN_EN control.

HDMI_FRUN_EN, Address 44 (CP), Address 0xBA[0]

HDMI_FRUN_EN is a control to enable free run in HDMI mode.

Table 290. HDMI_FRUN_EN Function Description

HDMI_FRUN_EN	Description
0	Disable the free run feature in HDMI mode
1 (default)	Enable the free run feature in HDMI mode

HDMI_FRUN_MODE, Address 44 (CP), Address 0xBA[1]

HDMI_FRUN_MODE is a control to configure the free run feature in HDMI mode.

Table 291. HDMI_FRUN_MODE Function Description

HDMI_FRUN_MODE	Description
0 (default)	HDMI Free Run Mode 0. The part free runs when the TMDS clock is not detected on the selected HDMI port.
1	HDMI Free Run Mode 1. The CP core free runs when the TMDS clock is not detected on the selected HDMI port or it the video resolution of HDMI stream processed by the part does not match the video resolution programmed in PRIM_MODE[3:0] and VID_STD[5:0].

DIS_AUTO_PARAM_BUFF, Address 44 (CP), Address 0xC9[0]

DIS_AUTO_PARAM_BUFF is a control to disable the buffering of the timing parameters used for free run in HDMI mode.

Table 292. DIS_AUTO_PARAM_BUFF Function Description

DIS_AUTO_PARAM_BUFF	Description
0 (default)	Buffer the last measured parameters in HDMI mode used to determine video resolution the part free runs into.
1	Disable the buffering of measured parameters in HDMI mode. Free run standard determined by PRIM_MODE[3:0], VID_STD[5:0], and V_FREQ[2:0]

It is also possible to custom program the resolution that the ADV7613 must expect for Free Run Mode 1 by programming the free run line length, line count max, and interlaced registers. See the Free Run Mode section for the configuration of these registers.

Note that this mode (that is, DIS_AUTOPARAM_BUFFER = 1) does not support HDMI input with deep color.

Free Run Default Color Output

In the event of loss of input signal, the ADV7613 may enter free run and can be configured to output a default color rather than noise. The default color values are given in Table 293.

The times at which the default colors are inserted can be set as follows:

- Free run is forced: default colors are always output.
- Automatic free run mode: default colors are output when the system detects a loss of video signal.

Table 293. Default Color Output Values (CP)

Mode	CP_DEF_COL_MAN_VAL	Signal	Value
Default—GR	0	CH_A (G) CH_B (R) CH_C (B)	0 0 135_d
Default—COMP	0	CH_A (Y) CH_A (Pr) CH_A (Pb)	35_d 114_d 212_d
Manual Override	1	CH_A CH_B CH_C	4·DEF_COL_CHA[7:0] 4·DEF_COL_CHB[7:0] 4·DEF_COL_CHC[7:0]

CP_FORCE_FREERUN, Address 44 (CP), Address 0xBF[0]

CP_FORCE_FREERUN is a control to force the CP to free run.

Table 294. CP_FORCE_FREERUN Function Description

CP_FORCE_FREERUN	Description
0 (default)	Do not force the CP core free run.
1	Force the CP core to free run.

CP_DEF_COL_AUTO, Address 44 (CP), Address 0xBF[1]

CP_DEF_COL_AUTO is a control to enable the insertion of default color when the CP free runs.

Table 295. CP_DEF_COL_AUTO Function Description

CP_DEF_COL_AUTO	Description
0	Disable automatic insertion of default color
1 (default)	Output default colors when the CP free runs

CP_DEF_COL_MAN_VAL, Address 44 (CP), Address 0xBF[2]

CP_DEF_COL_MAN_VAL is a control to enable manual selection of the color used when the CP core free runs.

Table 296. CP_DEF_COL_MAN_VAL Function Description

CP_DEF_COL_MAN_VAL	Description
0 (default)	Uses default color blue
1	Outputs default colors as given in CP_DEF_COL_CHA, CP_DEF_COL_B and CP_DEF_COL_C

Table 293 shows the default colors for component and graphics based video. The values describe the color blue. Setting the CP_DEF_COL_MAN_VAL bit high enables the user to overwrite the default colors with the values given in DEF_COL_CHA[7:0], DEF_COL_CHB[7:0], and DEF_COL_CHC[7:0].

The three parameters DEF_COL_CHA[7:0], DEF_COL_CHB[7:0], and DEF_COL_CHC[7:0] allow the user to specify their own default values.

Note that CP_DEF_COL_MAN_VAL must be set high for the three parameters to be used. See Table 293 for more information on the automatic values.

DEF_COL_CHA[7:0], Address 44 (CP), Address 0xC0[7:0]

DEF_COL_CHA[7:0] is a control the sets the default color for Channel A. It is to be used if CP_DEF_COL_MAN_VAL is 1.

Table 297. DEF_COL_CHA[7:0] Function Description

DEF_COL_CHA[7:0]	Description
0x00 (default)	Default value

DEF_COL_CHB[7:0], Address 44 (CP), Address 0xC1[7:0]

DEF_COL_CHB[7:0] is a control to set the default color for Channel B. It is to be used if CP_DEF_COL_MAN_VAL is 1.

Table 298. DEF_COL_CHB[7:0] Function Description

DEF_COL_CHB[7:0]	Description
0x00 (default)	Default value

DEF_COL_CHC[7:0], Address 44 (CP), Address 0xC2[7:0]

DEF_COL_CHC[7:0] is a control to set the default color for Channel C. It is to be used if CP_DEF_COL_MAN_VAL is 1.

Table 299. DEF_COL_CHC[7:0] Function Description

DEF_COL_CHC[7:0]	Description
0x00 (default)	Default value

CP STATUS

CP_REG_FF

CP_REG_FF is a status register that contains status bits for the CP core. Register CP_REG_FF holds field: CP_FREE_RUN.

Table 300. CP_REG_FF Bit Description

CP_REG_FF Bit Number	Bit Name	Description
0	Reserved	Reserved
1	Reserved	Reserved
2	Reserved	Reserved
3	Reserved	Reserved
4	CP_FREE_RUN	CP is free running (no valid video signal found)
5	Reserved	Reserved
6	Reserved	Reserved
7	Reserved	Reserved

CP_FREE_RUN, Address 44 (CP), Address 0xFF[4] (Read Only)

This bit provides the component processor free run status.

Table 301. CP_FREE_RUN Function Description

CP_FREE_RUN	Description
0 (default)	The CP is not free running.
1	The CP is free running.

CP CORE BYPASSING

It is possible to bypass CP core completely with using following register. When OP_FORMAT_SEL is set to 0x94, 0x95, 0x96, or 0x54, CP_COMPLETE_BYPASS_IN_HDMI_MODE must be set to 0.

CP_COMPLETE_BYPASS_IN_HDMI_MODE, IO, Address 0xBF[0]

Table 302. CP_COMPLETE_BYPASS_IN_HDMI_MODE Function Description

CP_COMPLETE_BYPASS_IN_HDMI_MODE	Description
0	Normal mode
1	HDMI data directly fed to output bypassing CP completely, CP_CLK can be powered down

CONSUMER ELECTRONICS CONTROL

The consumer electronics control (CEC) module features the hardware required to behave as an initiator or a follower as per the specifications for a CEC device. The CEC module contains four main sections:

- Transmit section, CEC_TX
- Receive section, CEC_RX
- Clock generator section, CEC_CLK_GEN
- Antiglitch filter section, CEC_ANTI_GLITCH

The block diagram of the CEC module is shown in Figure 49.

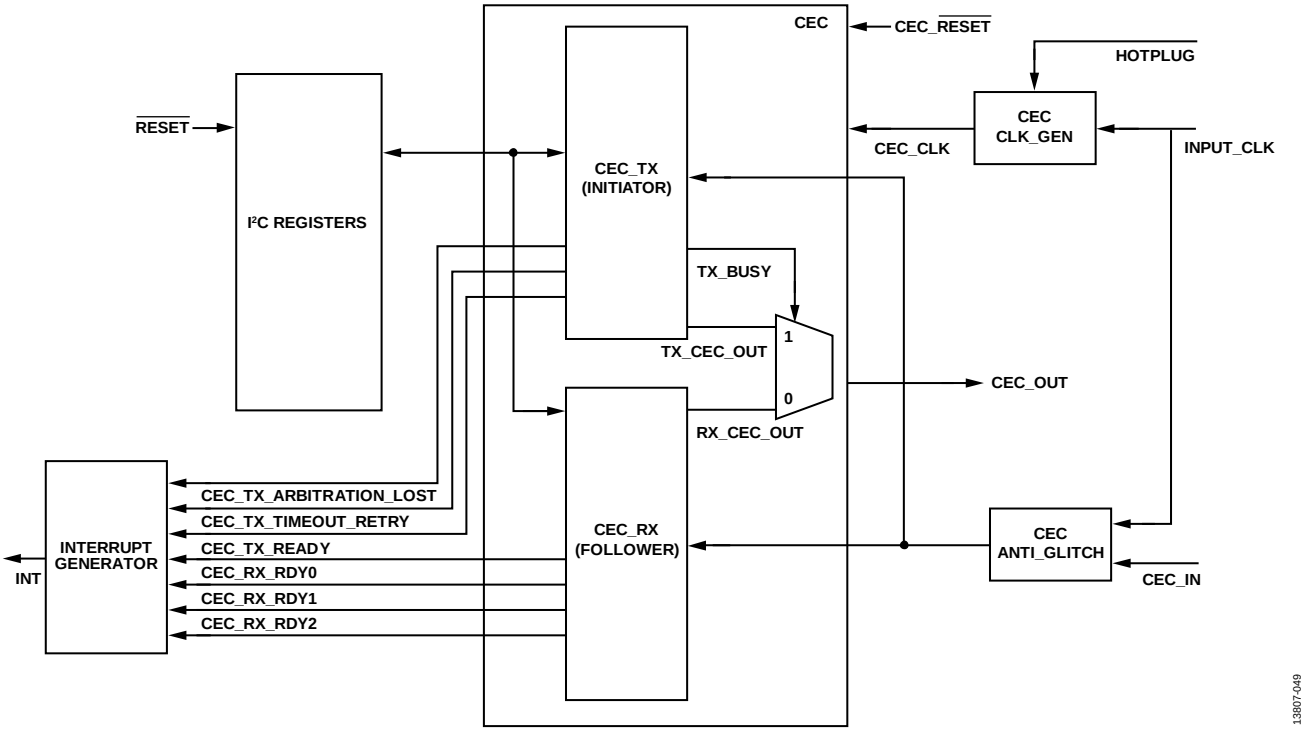

Figure 49. CEC Module Block Diagram

MAIN CONTROLS

This section describes the main controls for the CEC module.

CEC_POWER_UP, Address 80 (CEC), Address 0x2A[0]

This bit is the power mode of the CEC module.

Table 303. CEC_POWER_UP Function Description

CEC_POWER_UP	Description
0 (default)	Power down the CEC module
1	Power up the CEC module

CEC_SOFT_RESET, Address 80 (CEC), Address 0x2C[0] (Self Clearing)

This bit is the CEC module software reset.

Table 304. CEC_SOFT_RESET Function Description

CEC_SOFT_RESET	Description
0 (default)	No function
1	Reset the CEC module

Note that the CEC_POWER_UP bit can be used to set the ADV7613 to Power-Down Mode 1 (refer to the Power-Down Mode 1 section).

CEC TRANSMIT SECTION

The transmit section features the hardware required for the CEC module to act as an initiator. The host utilizes this section to transmit directly addressed messages or broadcast messages on the CEC bus. When the host wants to a send message to other CEC devices, it writes the message to the CEC outgoing message registers (refer to Table 305) and the message length register. Then, the host enables the transmission process by setting the CEC_TX_ENABLE bit to 1. When the message transmission is completed, or if an error occurs, the CEC transmitter section generates an interrupt (assuming the corresponding interrupt mask bits are set accordingly).

Table 305. CEC Outgoing Message Buffer Registers

Register Name	CEC Map Address	Description
CEC_TX_FRAME_HEADER[7:0]	0x00	Header of next outgoing message
CEC_TX_FRAME_DATA0[7:0]	0x01	Byte 0 of next outgoing message
CEC_TX_FRAME_DATA1[7:0]	0x02	Byte 1 of next outgoing message
CEC_TX_FRAME_DATA2[7:0]	0x03	Byte 2 of next outgoing message
CEC_TX_FRAME_DATA3[7:0]	0x04	Byte 3 of next outgoing message
CEC_TX_FRAME_DATA4[7:0]	0x05	Byte 4 of next outgoing message
CEC_TX_FRAME_DATA5[7:0]	0x06	Byte 5 of next outgoing message
CEC_TX_FRAME_DATA6[7:0]	0x07	Byte 6 of next outgoing message
CEC_TX_FRAME_DATA7[7:0]	0x08	Byte 7 of next outgoing message
CEC_TX_FRAME_DATA8[7:0]	0x09	Byte 8 of next outgoing message
CEC_TX_FRAME_DATA9[7:0]	0x0A	Byte 9 of next outgoing message
CEC_TX_FRAME_DATA10[7:0]	0x0B	Byte 10 of next outgoing message
CEC_TX_FRAME_DATA11[7:0]	0x0C	Byte 11 of next outgoing message
CEC_TX_FRAME_DATA12[7:0]	0x0D	Byte 12 of next outgoing message
CEC_TX_FRAME_DATA13[7:0]	0x0E	Byte 13 of next outgoing message
CEC_TX_FRAME_DATA14[7:0]	0x0F	Byte 14 of next outgoing message

CEC_TX_FRAME_LENGTH[4:0], Address 80 (CEC), Address 0x10[4:0]

CEC_TX_FRAME_LENGTH[4:0] is the message size of the transmitted frame. This is the number of byte in the outgoing message including the header.

Table 306. CEC_TX_FRAME_LENGTH[4:0] Function Description

CEC_TX_FRAME_LENGTH[4:0]	Description
xxxxx	Total number of bytes (including header byte) to be sent

CEC_TX_ENABLE, Address 80 (CEC), Address 0x11[0]

This bit enables the Tx section. When set to 1, it initiates the start of transmission of the message in the outgoing message buffer. When the message transmission is completed, this bit is automatically reset to 0. If it is manually set to 0 during a message transmission, it may terminate the transmission depending on what stage of the transmission process has been reached. If the message transmission is still in the signal free time stage, the message transmission is terminated. If data transmission has begun, the transmission continues until the message is fully sent, or until an error condition occurs.

Table 307. CEC_TX_ENABLE Function Description

CEC_TX_ENABLE	Description
0 (default)	Transmission mode disabled
1	Transmission mode enabled and message transmission started

The ADV7613 features three status bits related to the transmission of CEC messages. The events that set these bits are mutually exclusive, that is, only one of the three events can occur during any given message transmission: CEC_TX_READY_ST, CEC_TX_ARBITRATION_LOST_ST, and CEC_TX_RETRY_TIMEOUT_ST.

CEC_TX_READY_ST, IO, Address 0x93[0] (Read Only)

Latched status of CEC_TX_READY_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When the CEC TX successfully sends the current message, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_TX_READY_CLR.

Table 308. CEC_TX_READY_ST Function Description

CEC_TX_READY_ST	Description
0 (default)	No change
1	Message transmitted successfully

CEC_TX_ARBITRATION_LOST_ST, IO, Address 0x93[1] (Read Only)

Latched status of CEC_TX_ARBITRATION_LOST_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the CEC TX loses arbitration while trying to send a message, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_TX_ARBITRATION_LOST_CLR.

Table 309. CEC_TX_ARBITRATION_LOST_ST Function Description

CEC_TX_ARBITRATION_LOST_ST	Description
0 (default)	No change
1	The CEC TX has lost arbitration to another TX

CEC_TX_RETRY_TIMEOUT_ST, IO, Address 0x93[2] (Read Only)

Latched status of CEC_TX_RETRY_TIMEOUT_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the CEC TX fails to send the current message within the number of retry attempts specified by CEC_TX_RETRY this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_TX_RETRY_TIMEOUT_CLR.

Table 310. CEC_TX_RETRY_TIMEOUT_ST Function Description

CEC_TX_RETRY_TIMEOUT_ST	Description
0 (default)	No change
1	CEC TX has tried but failed to resend the current message for the number of times specified by CEC_TX_RETRY

CEC_TX_RETRY[2:0], Address 80 (CEC), Address 0x12[6:4]

CEC_TX_RETRY[2:0] is the number of times the CEC Tx must try to retransmit the message if an error condition is encountered. Per the CEC specification, this value must not be set to a value greater than 5.

Table 311. CEC_TX_RETRY[2:0] Function Description

CEC_TX_RETRY[2:0]	Description
001 (default)	Try to retransmit the message 1 time if an error occurs

CEC_TX_NACK_COUNTER[3:0], Address 80 (CEC), Address 0x14[3:0] (Read Only)

CEC_TX_NACK_COUNTER[3:0] is the number of times that the no acknowledge error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1.

Table 312. CEC_TX_NACK_COUNTER[3:0] Function Description

CEC_TX_NACK_COUNTER[3:0]	Description
0000 (default)	No error condition

CEC_TX_LOWDRIVE_COUNTER[3:0], Address 80 (CEC), Address 0x14[7:4] (Read Only)

CEC_TX_LOWDRIVE_COUNTER[3:0] is the number of times that the LOWDRIVE error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1.

Table 313. CEC_TX_LOWDRIVE_COUNTER[3:0] Function Description

CEC_TX_LOWDRIVE_COUNTER[3:0]	Description
0000 (default)	No error condition

CEC RECEIVE SECTION

The receive section features the hardware required for the CEC module to act as a follower. Once the CEC module is powered up via the CEC_POWER_UP bit, the CEC receiver (Rx) section immediately begins monitoring the CEC bus for messages with the correct logical address(es). When the message reception is completed, the CEC receive section generates an interrupt (assuming the corresponding interrupt mask bits are set accordingly).

The host can disable message reception while keeping the CEC module powered up by using the FORCE_NACK bit to not acknowledge received messages.

CEC_FORCE_NACK, Address 80 (CEC), Address 0x27[1]

CEC_FORCE_NACK forces no acknowledge control. Setting this bit forces the CEC controller not acknowledge any received messages.

Table 314. CEC_FORCE_NACK Function Description

CEC_FORCE_NACK	Description
0 (default)	Acknowledge received messages
1	Do not acknowledge received messages

Logical Address Configuration

The host must set the destination logical address(es) that the CEC receive section responds to. Up to three logical addresses can be enabled allowing support for multifunction devices such as DVD recorders with TV tuners, which require multiple logical addresses. The logical address(es) are set via the following registers:

- CEC_LOGICAL_ADDRESS2[3:0] if CEC_LOGICAL_ADDRESS_MASK[2] is set to 1
- CEC_LOGICAL_ADDRESS1[3:0] if CEC_LOGICAL_ADDRESS_MASK[1] is set to 1
- CEC_LOGICAL_ADDRESS0[3:0] if CEC_LOGICAL_ADDRESS_MASK[0] is set to 1

CEC_LOGICAL_ADDRESS2[3:0], Address 80 (CEC), Address 0x29[3:0]

CEC_LOGICAL_ADDRESS2[3:0] is Logical Address 2. This address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[2] to 1.

Table 315. CEC_LOGICAL_ADDRESS2[3:0] Function Description

CEC_LOGICAL_ADDRESS2[3:0]	Description
1111 (default)	Default value
xxxx	User specified logical address

CEC_LOGICAL_ADDRESS1[3:0], Address 80 (CEC), Address 0x28[7:4]

CEC_LOGICAL_ADDRESS1[3:0] is Logical Address 1. This address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[1] to 1.

Table 316. CEC_LOGICAL_ADDRESS1[3:0] Function Description

CEC_LOGICAL_ADDRESS1[3:0]	Description
1111 (default)	Default value
xxxx	User specified logical address

CEC_LOGICAL_ADDRESS0[3:0], Address 80 (CEC), Address 0x28[3:0]

CEC_LOGICAL_ADDRESS0[3:0] is Logical Address 0. This address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[0] to 1.

Table 317. CEC_LOGICAL_ADDRESS0[3:0] Function Description

CEC_LOGICAL_ADDRESS0[3:0]	Description
1111 (default)	Default value
xxxx	User specified logical address

CEC_LOGICAL_ADDRESS_MASK[2:0], Address 80 (CEC), Address 0x27[6:4]

CEC_LOGICAL_ADDRESS_MASK[2:0] is the logical address mask of the CEC logical devices. Up to three logical devices are supported. When the mask bits are set for a particular logical device, the logical device is enabled and messages whose destination address matches that of the selected logical address are accepted.

Table 318. CEC_LOGICAL_ADDRESS_MASK[2:0] Function Description

CEC_LOGICAL_ADDRESS_MASK[2:0]	Description
4	Mask bit for Logical Device 0
5	Mask bit for Logical Device 1
6	Mask bit for Logical Device 2

Receive Buffers

The ADV7613 features three frame buffers that allow the receiver to receive up to three messages before the host processor needs to read a message out. When three messages have been received, no further message reception is possible until the host reads at least one message.

Note that for backwards compatibility with previous generation Analog Devices CEC-enabled devices, only one frame buffer is enabled by default. In this default mode, after a message is received, the host processor must read the message out before any further message reception is possible. The decision to use one or three messages buffers is controlled by the CEC_USE_ALL_BUFS bit.

CEC_USE_ALL_BUFS, Address 80 (CEC), Address 0x77[0]

CEC_USE_ALL_BUFS is the control to enable supplementary receiver frame buffers.

Table 319. CEC_USE_ALL_BUFS Function Description

CEC_USE_ALL_BUFS	Description
0 (default)	Use only buffer 0 to store CEC frames
1	Use all 3 buffers to stores the CEC frames

For each of the frame buffers there is a corresponding two-bit time stamp and a raw flag.

CEC_BUF0_TIMESTAMP[1:0], Address 80 (CEC), Address 0x53[1:0] (Read Only)

CEC_BUF0_TIMESTAMP[1:0] is the time stamp for the frame stored in Receiver Frame Buffer 0. This can be used to determine which frame is to be read next from the receiver frame buffers.

Table 320. CEC_BUF0_TIMESTAMP[1:0] Function Description

CEC_BUF0_TIMESTAMP[1:0]	Description
00 (default)	Invalid timestamp, no frame is available in this frame buffer
01	Of the frames currently buffered, this frame was the first to be received
10	Of the frames currently buffered, this frame was the second to be received
11	Of the frames currently buffered, this frame was the third to be received

CEC_BUF1_TIMESTAMP[1:0], Address 80 (CEC), Address 0x53[3:2] (Read Only)

CEC_BUF1_TIMESTAMP[1:0] is the time stamp for the frame stored in Receiver Frame Buffer 1. This can be used to determine which frame must be read next from the receiver frame buffers.

Table 321. CEC_BUF1_TIMESTAMP[1:0] Function Description

CEC_BUF1_TIMESTAMP[1:0]	Description
00 (default)	Invalid timestamp, no frame is available in this frame buffer
01	Of the frames currently buffered, this frame was the first to be received
10	Of the frames currently buffered, this frame was the second to be received
11	Of the frames currently buffered, this frame was the third to be received

CEC_BUF2_TIMESTAMP[1:0], Address 80 (CEC), Address 0x53[5:4] (Read Only)

CEC_BUF2_TIMESTAMP[1:0] is the time stamp for the frame stored in Receiver Frame Buffer 2. This can be used to determine which frame must be read next from the receiver frame buffers.

Table 322. CEC_BUF2_TIMESTAMP[1:0] Function Description

CEC_BUF2_TIMESTAMP[1:0]	Description
00 (default)	Invalid timestamp, no frame is available in this frame buffer
01	Of the frames currently buffered, this frame was the first to be received
10	Of the frames currently buffered, this frame was the second to be received
11	Of the frames currently buffered, this frame was the third to be received

CEC_RX_RDY0_ST, IO, Address 0x93[3] (Read Only)

CEC_RX_RDY0_ST is the latched status of the CEC_RX_RDY0_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into Buffer 0, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_RX_RDY0_CLR.

Table 323. CEC_RX_RDY0_ST Function Description

CEC_RX_RDY0_ST	Description
0 (default)	No change
1	New CEC message received in Buffer 0

CEC_RX_RDY1_ST, IO, Address 0x93[4] (Read Only)

CEC_RX_RDY1_ST is the latched status of the CEC_RX_RDY1_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into Buffer 1, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_RX_RDY0_CLR.

Table 324. CEC_RX_RDY1_ST Function Description

CEC_RX_RDY1_ST	Description
0 (default)	No change
1	New CEC message received in Buffer 1

CEC_RX_RDY2_ST, IO, Address 0x93[5] (Read Only)

CEC_RX_RDY2_ST is the latched status of CEC_RX_RDY2_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into Buffer 2, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_RX_RDY0_CLR.

Table 325. CEC_RX_RDY2_ST Function Description

CEC_RX_RDY2_ST	Description
0 (default)	No change
1	New CEC message received in Buffer 2

When a message (other than a polling message) is received it is loaded into the first available frame buffer (starting with Buffer 0) and a 2-bit time stamp is generated for that buffer. If the corresponding interrupt mask bit is set the status bit relating to that buffer is set and an interrupt is generated to alert the host processor to the fact that a message has been received.

When all three frame buffers are full, the receive module can no longer receive CEC messages and does not acknowledge any new messages (other than polling messages). In the case that only one frame buffer is enabled (the default condition), only one message can be received. In this case, the received message is always available in Buffer 0.

The host can read the receive buffers (refer to Table 326, Table 329, and Table 332) to get the messages that were addressed to the CEC receiver. The length of each received message is available in the corresponding frame length register.

Table 326. CEC Incoming Frame Buffer 0 Registers

Register Name	CEC Map Address	Description
CEC_BUF0_RX_FRAME_HEADER[7:0]	0x15	Header of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA0[7:0]	0x16	Byte 0 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA1[7:0]	0x17	Byte 1 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA2[7:0]	0x18	Byte 2 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA3[7:0]	0x19	Byte 3 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA4[7:0]	0x1A	Byte 4 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA5[7:0]	0x1B	Byte 5 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA6[7:0]	0x1C	Byte 6 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA7[7:0]	0x1D	Byte 7 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA8[7:0]	0x1E	Byte 8 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA9[7:0]	0x1F	Byte 9 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA10[7:0]	0x20	Byte 10 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA11[7:0]	0x21	Byte 11 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA12[7:0]	0x22	Byte 12 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA13[7:0]	0x23	Byte 13 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA14[7:0]	0x24	Byte 14 of message in Frame Buffer 0

CEC_BUF0_RX_FRAME_LENGTH[4:0], Address 80 (CEC), Address 0x25[4:0] (Read Only)

Table 327. CEC_BUF0_RX_FRAME_LENGTH[4:0] Function Description

CEC_BUF0_RX_FRAME_LENGTH[4:0]	Description
xxxxx	The total number of bytes (including header byte) that were received into Buffer 0

CEC_CLR_RX_RDY0, Address 80 (CEC), Address 0x2C[1] (Self Clearing)

CEC_CLR_RX_RDY0 is the clear control for CEC_RX_RDY0.

Table 328. CEC_CLR_RX_RDY0 Function Description

CEC_CLR_RX_RDY0	Description
0 (default)	Retain the value of the CEC_RX_RDY0 flag
1	Clear the value of the CEC_RX_RDY0 flag

Table 329. CEC Incoming Frame Buffer 1 Registers

Register Name	CEC Map Address	Description
CEC_BUF1_RX_FRAME_HEADER[7:0]	0x54	Header of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA0[7:0]	0x55	Byte 0 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA1[7:0]	0x56	Byte 1 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA2[7:0]	0x57	Byte 2 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA3[7:0]	0x58	Byte 3 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA4[7:0]	0x59	Byte 4 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA5[7:0]	0x5A	Byte 5 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA6[7:0]	0x5B	Byte 6 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA7[7:0]	0x5C	Byte 7 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA8[7:0]	0x5D	Byte 8 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA9[7:0]	0x5E	Byte 9 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA10[7:0]	0x5F	Byte 10 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA11[7:0]	0x60	Byte 11 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA12[7:0]	0x61	Byte 12 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA13[7:0]	0x62	Byte 13 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA14[7:0]	0x63	Byte 14 of message in Frame Buffer 1

CEC_BUF1_RX_FRAME_LENGTH[4:0], Address 80 (CEC), Address 0x64[4:0] (Read Only)

Table 330. CEC_BUF1_RX_FRAME_LENGTH[4:0] Function Description

CEC_BUF1_RX_FRAME_LENGTH[4:0]	Description
xxxxx	The total number of bytes (including header byte) that were received into buffer 1

CEC_CLR_RX_RDY1, Address 80 (CEC), Address 0x2C[2] (Self Clearing)

Clear control for CEC_RX_RDY1.

Table 331. CEC_CLR_RX_RDY1 Function Description

CEC_CLR_RX_RDY1	Description
0 (default)	Retain the value of the CEC_ RX_RDY1 flag
1	Clear the value of the CEC_RX_RDY1 flag

Table 332. CEC Incoming Frame Buffer 2 Registers

Register Name	CEC Map Address	Description
CEC_BUF2_RX_FRAME_HEADER[7:0]	0x65	Header of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA0[7:0]	0x66	Byte 0 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA1[7:0]	0x67	Byte 1 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA2[7:0]	0x68	Byte 2 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA3[7:0]	0x69	Byte 3 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA4[7:0]	0x6A	Byte 4 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA5[7:0]	0x6B	Byte 5 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA6[7:0]	0x6C	Byte 6 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA7[7:0]	0x6D	Byte 7 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA8[7:0]	0x6E	Byte 8 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA9[7:0]	0x6F	Byte 9 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA10[7:0]	0x70	Byte 10 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA11[7:0]	0x71	Byte 11 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA12[7:0]	0x72	Byte 12 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA13[7:0]	0x73	Byte 13 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA14[7:0]	0x74	Byte 14 of message in Frame Buffer 2

CEC_BUF2_RX_FRAME_LENGTH[4:0], Address 80 (CEC), Address 0x75[4:0] (Read Only)

Table 333. CEC_BUF2_RX_FRAME_LENGTH[4:0] Function Description

CEC_BUF2_RX_FRAME_LENGTH[4:0]	Description
xxxxx	The total number of bytes (including header byte) that were received into buffer 2

CEC_CLR_RX_RDY2, Address 80 (CEC), Address 0x2C[3] (Self Clearing)

CEC_CLR_RX_RDY2 is the clear control for CEC_RX_RDY2.

Table 334. CEC_CLR_RX_RDY2 Function Description

CEC_CLR_RX_RDY2	Description
0 (default)	Retain the value of the CEC_RX_RDY2 flag
1	Clear the value of the CEC_RX_RDY2 flag

CEC Message Reception Overview

The following sequence describes how messages are received and stored when only one frame buffer is enabled (default condition).

1. Initially, the receive buffer (Buffer 0) is empty.
2. A message is received and stored in Receive Buffer 0, and CEC_BUF0_TIMESTAMP is set to 0b01. If the corresponding interrupt mask bit is set CEC_RX_RDY0_ST goes high and an interrupt is generated to alert the host processor that a message has been received. No more messages can be received until the processor reads out the received message.
3. The host processor responds to the interrupt, or polls the CEC_BUF0_TIMESTAMP register and realizes a message has been received, and reads Receive Buffer 0. Once the message is read the processor sets CEC_RX_RDY0_CLR which resets the Buffer 0 timestamp to 0b00 and also clears the Buffer 0 status bit (if applicable). The CEC module is now ready to receive the next incoming message.

The following sequence describes how messages are received and stored, how the time stamps are generated, and what happens when the host reads a received message when all three frame buffers are enabled.

1. Initially all buffers are empty and all time stamps are 0b00.
2. A message is received and stored in Receive Buffer 0, and CEC_BUF0_TIMESTAMP is set to 0b01. If the corresponding interrupt mask bit is set CEC_RX_RDY0_ST goes high and an interrupt is generated to alert the host processor that a message has been received.
3. Another message is received and stored in Receive Buffer 1, and CEC_BUF1_TIMESTAMP is set to 0b10. If the corresponding interrupt mask bit is set CEC_RX_RDY1_ST goes high and an interrupt is generated to alert the host processor that a message has been received.
4. The host processor responds to the interrupts, or polls the timestamps and realizes that messages have been received, and reads the three time stamps to determine which receive buffer to read first. The buffer with the earliest time stamp must be read first; in this example, the processor must read Receive Buffer 0 first. Once the message has been read, the processor sets CEC_RX_RDY0_CLR, which resets the Buffer 0 timestamp to 0b00 and also clears the Buffer 0 status bit (if applicable).
5. Another message is received. The receiver module checks to see which of the three buffers are available, starting with Buffer 0. In this example, Buffer 0 has been read out already by the host processor and is available so the new message is stored in Receive Buffer 0. At this time the timestamp for Receive Buffer 1 is adjusted to 0b01 to show that it contains the first received message, and a timestamp of 0b10 is assigned to Receive Buffer 0 to show that it contains the second received message. If the corresponding interrupt mask bit is set the CEC_RX_RDY0_ST bit goes high and an interrupt is generated to alert the host processor that a message has been received.
6. Another message is received. This message is stored in Receive Buffer 2 (Buffer 0 and Buffer 1 are full). Time stamp 0b11 is assigned to Receive Buffer 2 to show that it contains an unread message that was the third to be received. If the corresponding interrupt mask bit is set the CEC_RX_RDY2_ST bit goes high and an interrupt is generated to alert the host processor that a message has been received. At this time all receive buffers are full and no more messages can be received until the processor reads at least one message.
7. The host processor responds to the interrupts, or polls the timestamps and realizes that messages have been received, and reads the three time stamps. The buffer with the earliest time stamp must be read first, therefore Receive Buffer 1 is read first, followed by Receive Buffer 0 and then Receive Buffer 2. Once the messages are read the processor sets CEC_RX_RDY0_CLR, CEC_RX_RDY1_CLR, and CEC_RX_RDY2_CLR. The time stamps for all three buffers are reset to 0b00.

ANTIGLITCH FILTER MODULE

This module is used to remove any glitches on the CEC bus to make the CEC input signal cleaner before it enters the CEC module. The glitch filter is programmable through the CEC_GLITCH_FILTER_CTRL register. The register value specifies the minimum pulse width that is passed through by the module. Any pulses with narrower widths are rejected. There is a CEC_GLITCH_FILTER_CTRL + 1 number of clock delays introduced by the antiglitch filter.

CEC_GLITCH_FILTER_CTRL[5:0], Address 80 (CEC), Address 0x2B[5:0]

The CEC input signal is sampled by the input clock (XTAL clock). CEC_GLITCH_FILTER_CTRL specifies the minimum pulse width requirement in input clock cycles. Pulses of widths less than the minimum specified width are considered glitches and are removed by the filter.

Table 335. CEC_GLITCH_FILTER_CTRL[5:0] Function Description

CEC_GLITCH_FILTER_CTRL[5:0]	Description
000000	Disable the glitch filter
000001	Filter out pulses with width less than 1 clock cycle
000010	Filter out pulses with width less than 2 clock cycles
…	…
000111 (default)	Filter out pulses with width less than 7 clock cycles
…	…
111111	Filter out pulses with width less than 63 clock cycles

TYPICAL OPERATION FLOW

This section describes the algorithm that must be implemented in the host processor controlling the CEC module.

Initializing CEC Module

Figure 50 shows the flow that can be implemented in the host processor controlling the ADV7613 to initialize the CEC module.

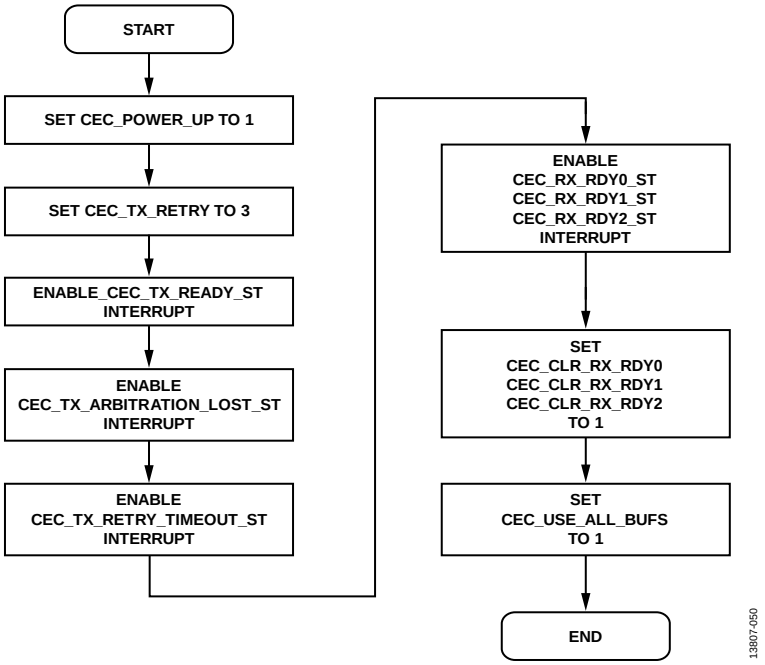

Figure 50. CEC Module Initialization

Using CEC Module as Initiator

Figure 51 shows the algorithm that can be implemented in the host processor controlling the ADV7613 to use the CEC module as an initiator.

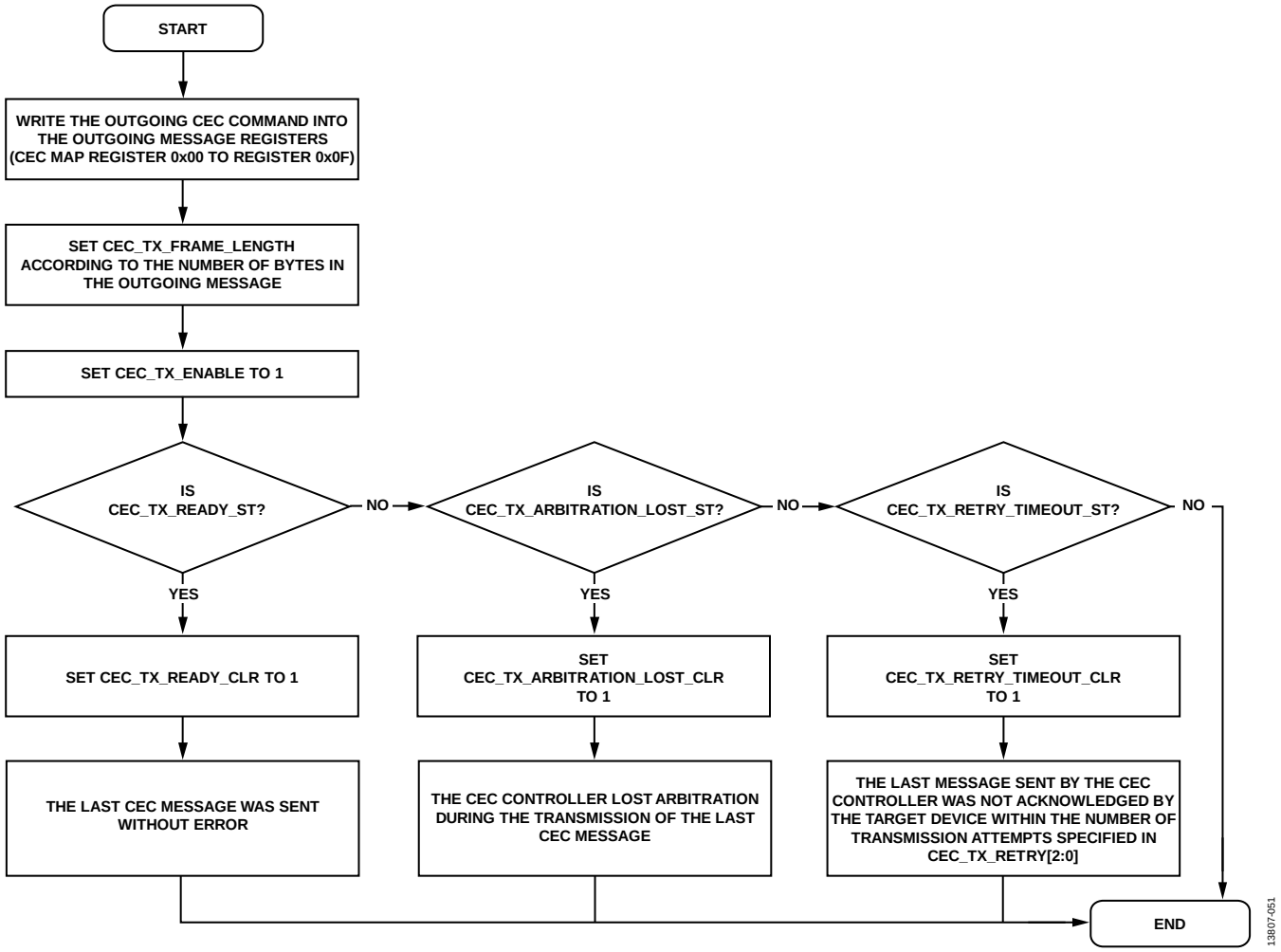

Figure 51. Using CEC Module as Initiator

Using CEC Module as Follower

Figure 52 shows the algorithm that can be implemented in the host processor controlling the ADV7613 to use the CEC module as a follower.

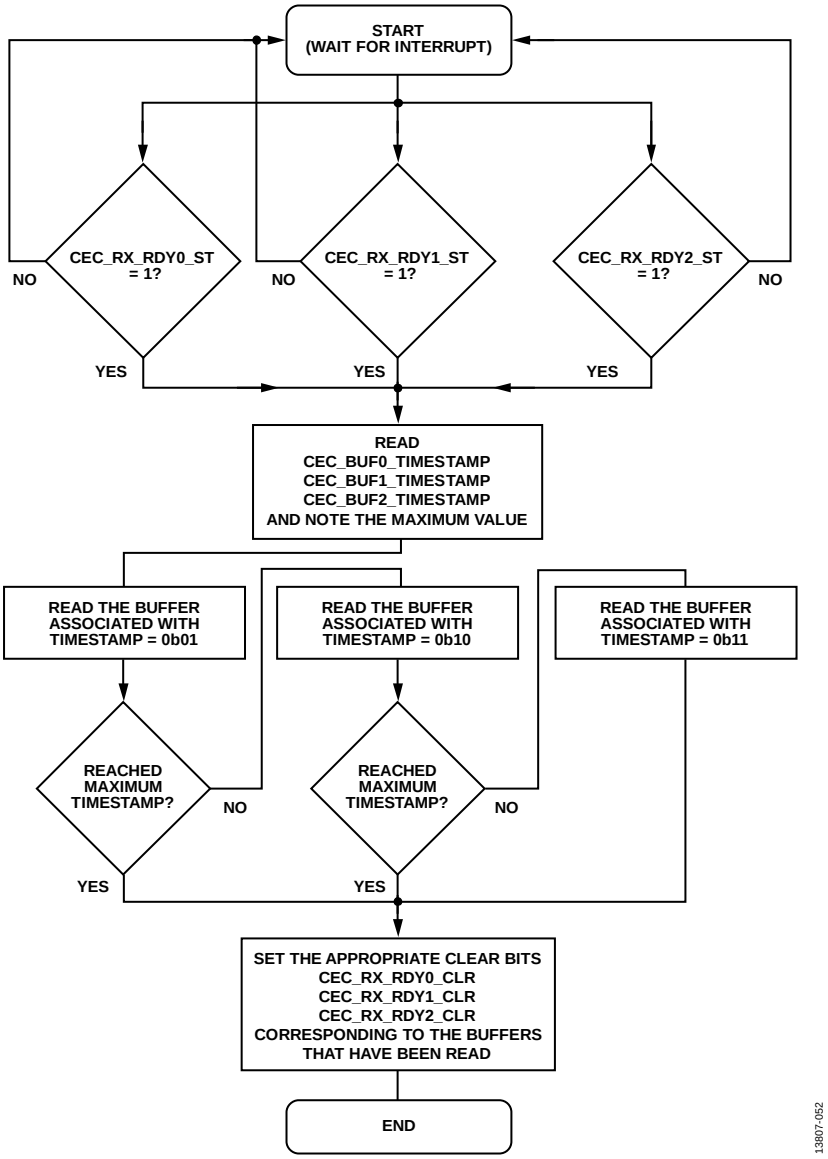

Figure 52. Using CEC Module as Follower

LOW POWER CEC MESSAGE MONITORING

The ADV7613 can be programmed to monitor the CEC line for messages that contain specific, user-programmable opcodes. These are referred to as WAKE_OPCODEs, because they allow the system to go into a low power or sleep mode and be woken up when an opcode of interest is received, without the host processor having to check each received message.

The default values of the WAKE_OPCODE registers are detailed in this section. All of these registers can be overwritten as required by the host processor.

For each of the eight WAKE_OPCODE registers, there is a corresponding raw flag, a status bit and a clear bit. If one of the WAKE_OPCODEs is received the corresponding raw flag goes high for a brief period of time. If the appropriate interrupt mask bit is set, the status bit goes high and remains high until cleared by the clear bit, and an interrupt is also generated.

CEC_WAKE_OPCODE0[7:0], Address 80 (CEC), Address 0x78[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Table 336. CEC_WAKE_OPCODE0[7:0] Function Description

CEC_WAKE_OPCODE0[7:0]	Description
01101101 (default)	Power on
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE1[7:0], Address 80 (CEC), Address 0x79[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Table 337. CEC_WAKE_OPCODE1[7:0] Function Description

CEC_WAKE_OPCODE1[7:0]	Description
10001111 (default)	Give power status
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE2[7:0], Address 80 (CEC), Address 0x7A[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Table 338. CEC_WAKE_OPCODE2[7:0] Function Description

CEC_WAKE_OPCODE2[7:0]	Description
10000010 (default)	Active source
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE3[7:0], Address 80 (CEC), Address 0x7B[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Table 339. CEC_WAKE_OPCODE3[7:0] Function Description

CEC_WAKE_OPCODE3[7:0]	Description
00000100 (default)	Image view on
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE4[7:0], Address 80 (CEC), Address 0x7C[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Table 340. CEC_WAKE_OPCODE4[7:0] Function Description

CEC_WAKE_OPCODE4[7:0]	Description
00001101 (default)	Text view on
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE5[7:0], Address 80 (CEC), Address 0x7D[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Table 341. CEC_WAKE_OPCODE5[7:0] Function Description

CEC_WAKE_OPCODE5[7:0]	Description
01110000 (default)	System audio mode request
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE6[7:0], Address 80 (CEC), Address 0x7E[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Table 342. CEC_WAKE_OPCODE6[7:0] Function Description

CEC_WAKE_OPCODE6[7:0]	Description
01000010 (default)	Deck control
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE7[7:0], Address 80 (CEC), Address 0x7F[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Table 343. CEC_WAKE_OPCODE7[7:0] Function Description

CEC_WAKE_OPCODE7[7:0]	Description
01000001 (default)	Play
xxxxxxxx	User specified opcode to respond to

INTERRUPTS

INTERRUPT ARCHITECTURE OVERVIEW

The ADV7613 interrupt architecture provides four different types of bits:

- Raw bits
- Status bits
- Interrupt mask bits
- Clear bits

Raw bits are defined as being either edge-sensitive or level-sensitive. The following example compares AVI_INFO_RAW and NEW_AVI_INFO_RAW to demonstrate the difference.

AVI_INFO_RAW, IO, Address 0x60[0] (Read Only)

This bit is the raw status of AVI InfoFrame detected signal. This bit is set to one when an AVI InfoFrame is received and is reset to zero if no AVI InfoFrame is received for more than seven VSYNCs (on the eighth VSYNC leading edge following the last received AVI InfoFrame), after an HDMI packet detection reset or upon writing to AVI_PACKET_ID.

Table 344. AVI_INFO_RAW Function Description

AVI_INFO_RAW	Description
0 (default)	No AVI InfoFrame has been received within the last seven VSYNCs or since the last HDMI packet detection reset
1	An AVI InfoFrame has been received within the last seven VSYNCs

NEW_AVI_INFO_RAW, IO, Address 0x79[0] (Read Only)

This bit is the status of the new AVI InfoFrame interrupt signal. When set to 1, it indicates that an AVI InfoFrame has been received with new contents. Once set, this bit remains high until the interrupt is cleared via NEW_AVI_INFO_CLR.

Table 345. NEW_AVI_INFO_RAW Function Description

NEW_AVI_INFO_RAW	Description
0 (default)	No new AVI InfoFrame received
1	AVI InfoFrame with new content received

In the case of AVI_INFO_RAW, this bit always represents the current status of whether or not the part is receiving AVI InfoFrames. It is not a latched bit and never requires to be cleared. This is the definition of a level-sensitive raw bit.

In the case of NEW_AVI_INFO_RAW, the same strategy does not work. If the NEW_AVI_INFO_RAW bit behaves in the same way as AVI_INFO_RAW, it goes high at the instant the new InfoFrame is received, and goes low again some clock cycles later. This is because a new InfoFrame is only new the instant it is received, and once received, it is no longer new; therefore, the event to set this bit only last for an instant and is then gone.

Having a raw bit that is only held high for an instant is not useful. Therefore, for these types of events, the raw bit is latched, and must be cleared by the corresponding clear bit. Accordingly, the raw bit does not truly represent the current status; instead it represents the status of an edge event that happened in the past. This is the definition of an edge-sensitive raw bit.

All raw bits, with the exception of INTRQ_RAW have corresponding status bits. The status bits always work in the same manner whether the raw bit is edge or level sensitive. Status bits have the following characteristics:

- A status bit must be enabled by setting either or both of the corresponding interrupt mask bits
- Status bits are always latched, and must be cleared by the corresponding clear bit.

When either of the interrupt mask bits for a given interrupt is set, if that raw bit changes state the corresponding status bit goes high and an interrupt is generated on the INT1 pin, depending on which interrupt mask bit was set. The status bit must be cleared using the appropriate clear bit. The status bits, interrupt mask bits, and clear bits for AVI_INFO and NEW_AVI_INFO are described here for completeness.

AVI_INFO_ST, IO, Address 0x61[0] (Read Only)

Latched status of AVI_INFO_RAW signal. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit. Once set, this bit remains high until the interrupt is cleared via AVI_INFO_CLR.

Table 346. AVI_INFO_ST Function Description

AVI_INFO_ST	Description
0 (default)	AVI_INFO_RAW has not changed state
1	AVI_INFO_RAW has changed state

NEW_AVI_INFO_ST, IO, Address 0x7A[0] (Read Only)

NEW_AVI_INFO_ST is the latched status for the NEW_AVI_INFO_RAW. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit. Once set, this bit remains high until the interrupt is cleared via NEW_AVI_INFO_CLR.

Table 347. NEW_AVI_INFO_ST Function Description

NEW_AVI_INFO_ST	Description
0 (default)	NEW_AVI_INFO_RAW has not changed state
1	NEW_AVI_INFO_RAW has changed state

AVI_INFO_CLR, IO, Address 0x62[0] (Self Clearing)

AVI_INFO_CLR is the clear bit for AVI_INFO_RAW and AVI_INFO_ST bits.

Table 348. AVI_INFO_CLR Function Description

AVI_INFO_CLR	Description
0 (default)	No function
1	Clear AVI_INFO_RAW and AVI_INFO_ST

NEW_AVI_INFO_CLR, IO, Address 0x7B[0] (Self Clearing)

NEW_AVI_INFO_CLR is the clear bit for the NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST bits.

Table 349. NEW_AVI_INFO_CLR Function Description

NEW_AVI_INFO_CLR	Description
0 (default)	No function
1	Clear NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST

AVI_INFO_MB1, IO, Address 0x64[0]

AVI_INFO_MB1 is the INT1 interrupt mask for AVI InfoFrame detection interrupt. When set, an AVI InfoFrame detection event causes AVI_INFO_ST to be set and an interrupt is generated on INT1.

Table 350. AVI_INFO_MB1 Function Description

AVI_INFO_MB1	Description
0 (default)	Disables AVI Info frame detection interrupt for INT1
1	Enables AVI Info frame detection interrupt for INT1

NEW_AVI_INFO_MB1, IO, Address 0x7D[0]

NEW_AVI_INFO_MB1 is the INT1 interrupt mask for new AVI InfoFrame detection interrupt. When set, a new AVI InfoFrame detection event causes NEW_AVI_INFO_ST to be set and an interrupt is generated on INT1.

Table 351. NEW_AVI_INFO_MB1 Function Description

NEW_AVI_INFO_MB1	Description
0 (default)	Disables new AVI InfoFrame interrupt for INT1
1	Enables new AVI InfoFrame interrupt for INT1

See Figure 53 through Figure 55 for interrupt output generation.

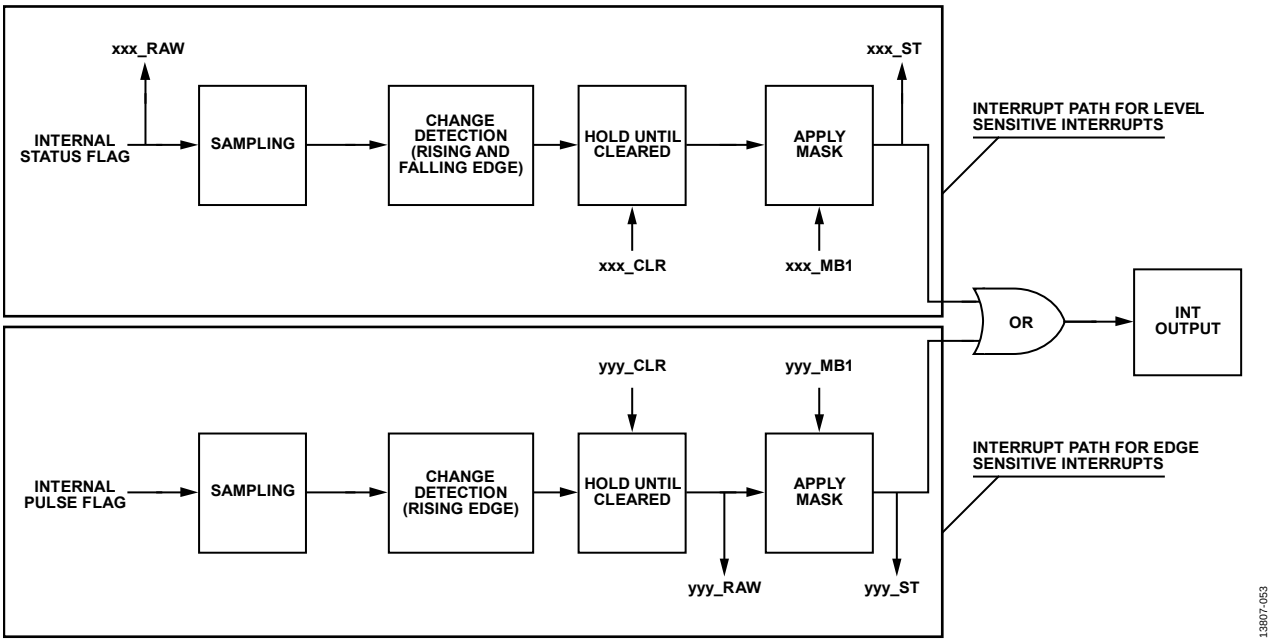

Figure 53. Level and Edge Sensitive Raw, Status, and Interrupt Generation

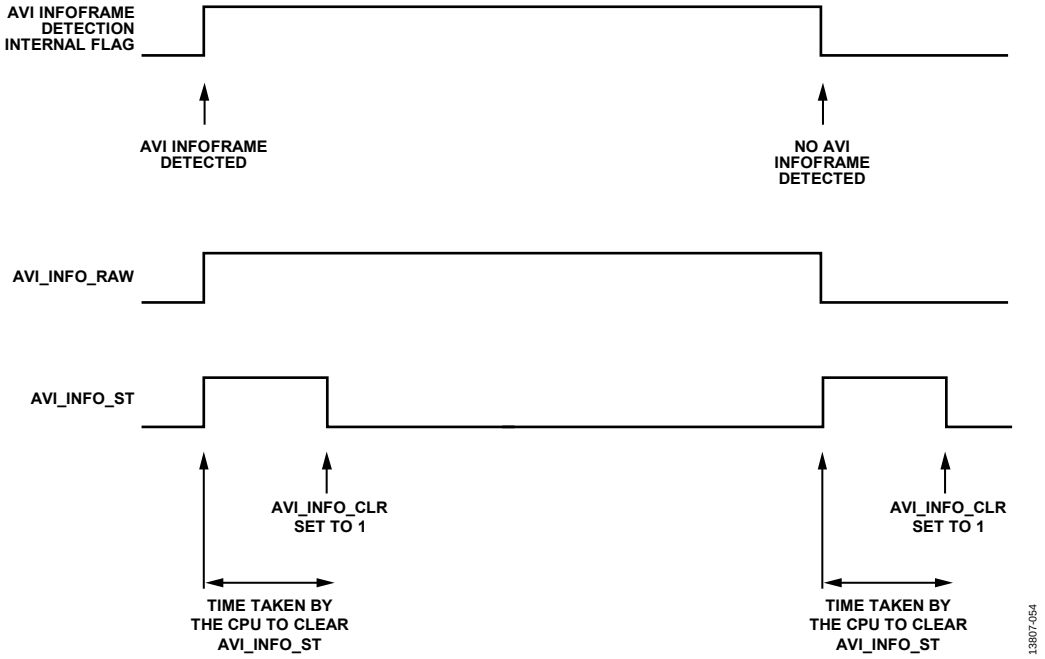

Figure 54. AVI_INFO_RAW and AVI_INFO_ST Timing

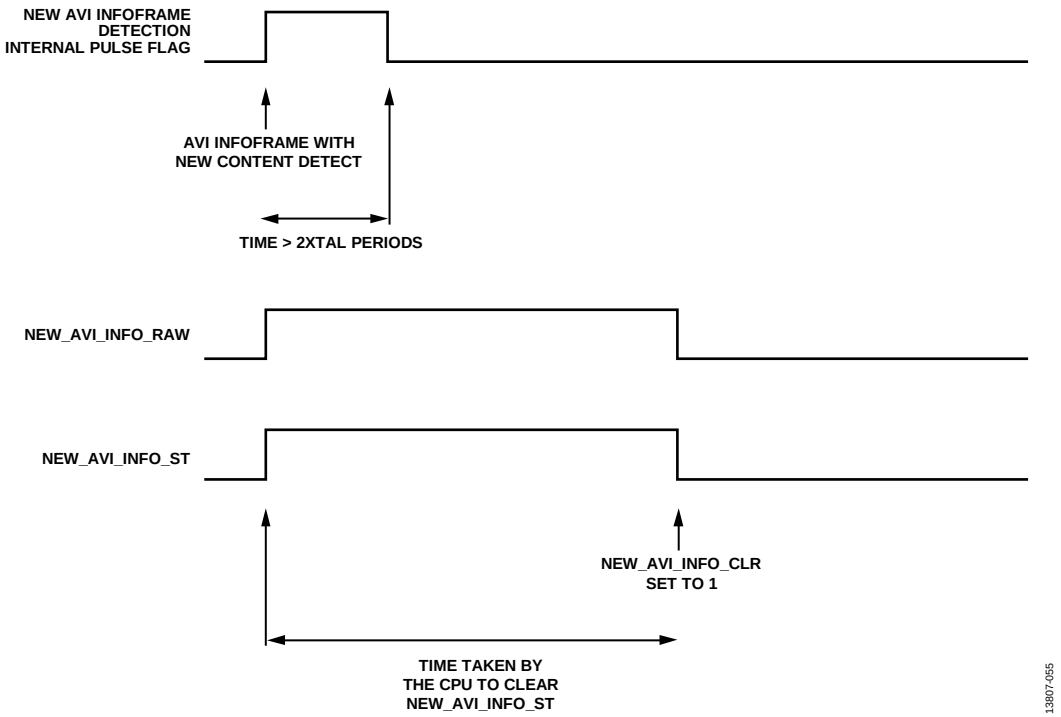

Figure 55. NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST Timing

In this section, all raw bits are classified as being triggered by either level sensitive or edge sensitive events, with the following understanding of the terminology.

Level sensitive events are events that are generally either high or low and are not expected to change rapidly. The raw bit for level sensitive events is not latched and therefore always represents the true real-time status of the event in question.

Edge sensitive events are events that only exist for an instant. The raw bits for edge sensitive events are latched and therefore represent the occurrence of an edge sensitive event that happened in the past. Raw bits for edge sensitive events must be cleared by the corresponding clear bit.

INTERRUPT PINS

The ADV7613 features one dedicated interrupt pin, INT1. INT1 is always enabled.

Note that the INT1 is in a high impedance state after reset because the ADV7613 resets with open drain enabled on INT1.

The ADV7613 resets with all interrupts masked off on INT1.

An interrupt is enabled for a specific event by masking the corresponding mask bit in the IO map.

Interrupt Duration

The interrupt duration can be programmed independently for INT1. When an interrupt event occurs, the interrupt pin INT1becomes active with a programmable duration, described as follows.

INTRQ_DUR_SEL[1:0], IO, Address 0x40[7:6]

INTRQ_DUR_SEL[1:0] is a control to select the interrupt signal duration for the interrupt signal on INT1.

Table 352. INTRQ_DUR_SEL[1:0] Function Description

INTRQ_DUR_SEL[1:0]	Description
00 (default)	4 XTAL periods
01	16 XTAL periods
10	64 XTAL periods
11	Active until cleared

Interrupt Drive Level

The drive level of INT1 and INT2 can be programmed as follows.

INTRQ_OP_SEL[1:0], IO, Address 0x40[1:0]

INTRQ_OP_SEL[1:0] is the interrupt signal configuration control for INT1.

Table 353. INTRQ_OP_SEL[1:0] Function Description

INTRQ_OP_SEL[1:0]	Description
00 (default)	Open drain
01	Drives low when active
10	Drives high when active
11	Disabled

Interrupt Manual Assertion

It is possible to manually generate an interrupt on the INT1 pin by setting MPU_STIM_INTRQ. This feature is designed for debug use and not intended for use in normal operation. The appropriate mask bit must be set to generate an interrupt at the pin.

MPU_STIM_INTRQ, IO, Address 0x40[2]

MPU_STIM_INTRQ is the manual interrupt set control. Use this feature for test purposes only. Note that the appropriate mask bit must be set to generate an interrupt at the pin.

Table 354. MPU_STIM_INTRQ Function Description

MPU_STIM_INTRQ	Description
0 (default)	Disables manual interrupt mode
1	Enables manual interrupt mode

MPU_STIM_INTRQ_MB1, IO, Address 0x4B[7]

MPU_STIM_INTRQ_MB1 is the INT1 interrupt mask for manual forced interrupt signal. When set, the manual forced interrupt triggers the INT1 interrupt, and MPU_STIM_INTRQ_ST indicates the interrupt status.

Table 355. MPU_STIM_INTRQ_MB1 Function Description

MPU_STIM_INTRQ_MB1	Description
0 (default)	Disables manual forced interrupt for INT1
1	Enables manual forced interrupt for INT1

Multiple Interrupt Events

If an interrupt event occurs, and then a second interrupt event occurs before the system controller has cleared or masked the first interrupt event, the ADV7613 does not generate a second interrupt signal. The system controller must check all unmasked interrupt status bits as more than one may be active.

Table 356 lists the interrupt registers available and a brief description of their functions. For more details on the functionality of these interrupt registers, see the ADV7613 Register Control Manual. Refer to the IO Register Map section of the ADV7613 Register Control Manual for details of the CP core interrupts and HDMI core interrupts.

Table 356. Interrupt Functions Available in ADV7613

Interrupt Register	Location	Description
Interrupt Status 1	IO Map, Address 0x43	CP interrupt status for STDI
Interrupt Status 2	IO Map, Address 0x48	CP interrupt status forces manual interrupt
Interrupt Status 6	IO Map, Address 0x5C	STDI channels interrupt status
HDMI Level Interrupt Status 1	IO Map, Address 0x61	HDMI interrupt status for HDMI InfoFrame packets
HDMI Level Interrupt Status 2	IO Map, Address 0x66	HDMI interrupt status for audio processing changes
HDMI Level Interrupt Status 3	IO Map, Address 0x6B	HDMI interrupt status for HDMI video parameters and cable detection
HDMI Level Interrupt Status 4	IO Map, Address 0x70	HDMI interrupt status for cable detection and encryption
HDMI Edge Interrupt Status 1	IO Map, Address 0x7A	HDMI interrupt status for newly received HDMI InfoFrame packets
HDMI Edge Interrupt Status 2	IO Map, Address 0x7F	HDMI interrupt status for audio FIFO, clock regeneration and packet errors
HDMI Edge Interrupt Status 3	IO Map, Address 0x84	HDMI interrupt status for updates in deep color, video, AKSV, and audio
HDMI Edge Interrupt Status 4	IO Map, Address 0x89	HDMI interrupt status for changes in InfoFrame checksum errors
HDMI Edge Interrupt Status 5	IO Map, Address 0x8E	HDMI interrupt status for background measurements and changes in InfoFrame checksum error

DESCRIPTION OF INTERRUPT BITS

This section lists all the raw bits in the IO map of the ADV7613 by category, and states whether the bit is an edge or level sensitive bit. A basic explanation for each bit is provided in the software manual and/or in the corresponding section of the hardware manual. For certain interrupts that require additional explanations, these explanations are provided in the Additional Explanations section.

General Operation

The following are general operation bits:

- INTRQ_RAW (level sensitive event)
- MPU_STIM_INTRQ_RAW (edge sensitive event)

HDMI Video Mode

The following are HDMI video mode bits:

- STDI_DATA_VALID_RAW (edge/level sensitive event; programmable).
- STDI_DVALID_CH1_RAW (edge/level sensitive event; programmable). Edge sensitive event on ADV7613.
- CP_UNLOCK_RAW (edge/level sensitive event; programmable). Edge sensitive event on ADV7613.
- CP_UNLOCK_CH1_RAW (edge/level sensitive event; programmable). Edge sensitive event on ADV7613.
- CP_LOCK_RAW (edge/level sensitive event; programmable). Edge sensitive event on ADV7613.
- CP_LOCK_CH1_RAW (edge/level sensitive event; programmable). Edge sensitive event on ADV7613.

CEC

The following raw bits are all related to CEC operation and are all edge sensitive events; it is, therefore, necessary to clear these bits.

- CEC_RX_RDY2_RAW
- CEC_RX_RDY1_RAW
- CEC_RX_RDY0_RAW
- CEC_TX_RETRY_TIMEOUT_RAW
- CEC_TX_ARBITRATION_LOST_RAW
- CEC_TX_READY_RAW
- CEC_INTERRUPT_BYTE[7:0]

HDMI Only Mode

The following raw bits are all related to HDMI operation and are based on level sensitive events; it is, therefore, not necessary to clear these bits.

- ISRC2_PCKT_RAW
- ISRC1_PCKT_RAW
- ACP_PCKT_RAW
- VS_INFO_RAW
- MS_INFO_RAW
- SPD_INFO_RAW
- AUDIO_INFO_RAW
- AVI_INFO_RAW
- CS_DATA_VALID_RAW
- INTERNAL_MUTE_RAW
- AV_MUTE_RAW
- AUDIO_CH_MD_RAW
- HDMI_MODE_RAW
- GEN_CTL_PCKT_RAW
- AUDIO_C_PCKT_RAW
- GAMUT_MDATA_RAW
- TMDSPLL_LCK_A_RAW
- TMDS_CLK_A_RAW
- HDMI_ENCRPT_A_RAW
- CABLE_DET_A_RAW
- V_LOCKED_RAW
- DE_REGEN_LCK_RAW
- VIDEO_3D_RAW
- RI_EXPIRED_A_RAW

The following raw bits are all related to HDMI operation and are based on edge sensitive events; it is, therefore, necessary to clear these bits using the corresponding clear bit.

- NEW_ISRC2_PCKT_RAW
- NEW_ISRC1_PCKT_RAW
- NEW_ACP_PCKT_RAW
- NEW_VS_INFO_RAW
- NEW_MS_INFO_RAW
- NEW_SPD_INFO_RAW
- NEW_AUDIO_INFO_RAW
- NEW_AVI_INFO_RAW
- NEW_GAMUT_MDATA_RAW
- FIFO_NEAR_OVFL_RAW
- FIFO_NEAR_UFLO_RAW
- FIFO_UNDERFLO_RAW
- FIFO_OVERFLO_RAW
- CTS_PASS_THRSH_RAW
- CHANGE_N_RAW
- PACKET_ERROR_RAW
- AUDIO_PCKT_ERR_RAW
- DEEP_COLOR_CHNG_RAW
- VCLK_CHNG_RAW
- AUDIO_MODE_CHNG_RAW
- PARITY_ERROR_RAW

- NEW_SAMP_RT_RAW
- AUDIO_FLT_LINE_RAW
- NEW_TMDS_FRQ_RAW
- MS_INF_CKS_ERR_RAW
- SPD_INF_CKS_ERR_RAW
- AUD_INF_CKS_ERR_RAW
- AVI_INF_CKS_ERR_RAW
- AKSV_UPDATE_A_RAW
- BG_MEAS_DONE_RAW
- VS_INF_CKS_ERR_RAW

ADDITIONAL EXPLANATIONS

STDI_DATA_VALID_RAW

STDI_DATA_VALID_RAW is programmable as either an edge sensitive bit or a level sensitive bit using the following control. Note that this control also configures whether an interrupt is generated only on the rising edge of STDI_DATA_VALID_RAW or on both edges.

STDI_DATA_VALID_EDGE_SEL, IO, Address 0x41[4]

This bit is a control to configure the functionality of the STDI_DATA_VALID interrupt. The interrupt can be generated for when STDI changes to an STDI valid state. Alternatively, it can be generated to indicate a change in STDI_VALID status.

Table 357. STDI_DATA_VALID_EDGE_SEL Function Description

STDI_DATA_VALID_EDGE_SEL	Description
0	Generate interrupt for a low to high change in STDI_VALID status
1 (default)	Generate interrupt for a low to high or a high to low change in STDI_VALID status

CP_LOCK, CP_UNLOCK

CP_UNLOCK_RAW is programmable as either an edge sensitive bit or a level sensitive bit using the following control. Note that this control also configures whether an interrupt is generated only on the rising edge of CP_UNLOCK_RAW, or on both edges.

CP_LOCK_UNLOCK_EDGE_SEL, IO, Address 0x41[5]

This bit is a control to configure the functionality of the CP_LOCK, CP_UNLOCK interrupts.

Table 358. CP_LOCK_UNLOCK_EDGE_SEL Function Description

CP_LOCK_UNLOCK_EDGE_SEL	Description
0	Generate interrupt for a low to high change in CP_LOCK,UNLOCK status for Ch1.
1 (default)	Generate interrupt for a low to high or a high to low change in CP_LOCK,UNLOCK status for Ch1.

CP_LOCK_ST, IO, Address 0x43[2] (Read Only)

For a detailed description of this function, see the entry in the List of Interrupt Status Registers section.

CP_UNLOCK_ST, IO, Address 0x43[3] (Read Only)

For a detailed description of this function, see the entry in the List of Interrupt Status Registers section.

HDMI Interrupts Validity Checking Process

All HDMI interrupts have a set of conditions that must be taken into account for validation in the display firmware. When the ADV7613 interrupts the display controller for an HDMI interrupt, the host must check that all validity conditions for that interrupt are met before processing that interrupt.

For simplicity, HDMI interrupts can be subdivided into three groups, as listed in the following sections.

Group 1 HDMI Interrupts

The following interrupts are valid irrespective of the mode in which the ADV7613 is configured, that is, HDMI mode (PRIM_MODE set to values of 0x05 or 0x06).

- TMDS_CLK_A
- CABLE_DET_A

Group 2 HDMI Interrupts

The following interrupts are valid on the condition that the ADV7613 is configured in HMDI mode.

- INTERNAL_MUTE
- VIDEO_PLL_LCK
- AKSV_UPDATE

Group 3 HDMI Interrupts

The following interrupts are valid under three conditions: the ADV7613 is configured in HMDI mode, TMDS_CLK_A_RAW is set to 1 if Port A is the active HDMI port, or TMDSPLL_LCK_A_RAW is set to 1.

- ISRC2_PCKT
- ISRC1_PCKT
- ACP_PCKT
- VS_INFO
- MS_INFO
- SPD_INFO
- AUDIO_INFO
- AVI_INFO
- CS_DATA_VALID
- AV_MUTE
- AUDIO_CH_MD
- AUDIO_MODE_CHNG
- GEN_CTL_PCKT
- AUDIO_C_PCKT
- GAMUT_MDATA
- V_LOCKED
- DE_REGEN_LCK
- HDMI_MODE
- HDMI_ENCRPT_A
- NEW_ISRC2_PCKT
- NEW_ISRC1_ PCKT
- NEW_ACP_PCKT
- NEW_VS_INFO
- NEW_MS_INFO
- NEW_SPD_INFO
- NEW_AUDIO_INFO
- NEW_AVI_INFO
- FIFO_NEAR_OVFL
- CTS_PASS_THRSH
- CHANGE_N
- PACKET_ERROR
- AUDIO_PCKT_ERR
- NEW_GAMUT_MDATA
- DEEP_COLOR_CHNG
- VCLK_CHNG
- PARRITY_ERROR
- NEW_SAMP_RT
- AUDIO_FLT_LINE
- NEW_TMDS_FRQ
- FIFO_NEAR_UFLO
- VIDEO_3D_RAW
- RI_EXPIRED_A_RAW

Storing Masked Interrupts

STORE_UNMASKED_IRQS, IO, Address 0x40[4]

STORE_MASKED_IRQS allows the HDMI status flags for any HDMI interrupt to be triggered regardless of whether the mask bits are set. This bit allows a HDMI interrupt to trigger and allows this interrupt to be read back through the corresponding status bit without triggering an interrupt on the interrupt pin. The status is stored until the clear bit is used to clear the status register and allows another interrupt to occur.

Table 359. STORE_UNMASKED_IRQS Function Description

STORE_UNMASKED_IRQS	Description
0 (default)	Does not allow x_ST flag of any HDMI interrupt to be set independently of mask bits
1	Allows x_ST flag of any HDMI interrupt to be set independently of mask bits

List of Interrupt Status Registers

The INTERRUPT_STATUS_1 register consists of the following fields: STDI_DATA_VALID_ST, CP_UNLOCK_ST, and CP_LOCK_ST.

STDI_DATA_VALID_ST, IO, Address 0x43[4] (Read Only)

STDI_DATA_VALID_ST is the latched signal status of STDI valid interrupt signal. Once set, this bit remains high until the interrupt is cleared via STDI_DATA_VALID_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 360. STDI_DATA_VALID_ST Function Description

STDI_DATA_VALID_ST	Description
0 (default)	No STDI valid interrupt has occurred.
1	A STDI valid interrupt has occurred.

CP_UNLOCK_ST, IO, Address 0x43[3] (Read Only)

CP_UNLOCK_ST is the latched signal status of CP Unlock interrupt signal. Once set, this bit remains high until the interrupt is cleared via CP_UNLOCK_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 361. CP_UNLOCK_ST Function Description

CP_UNLOCK_ST	Description
0 (default)	No CP UNLOCK interrupt event has occurred.
1	A CP UNLOCK interrupt event has occurred.

CP_LOCK_ST, IO, Address 0x43[2] (Read Only)

CP_LOCK_ST is the latched signal status of the CP lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via CP_LOCK_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 362. CP_LOCK_ST Function Description

CP_LOCK_ST	Description
0 (default)	No CP LOCK interrupt event has occurred.
1	A CP LOCK interrupt event has occurred.

The INTERRUPT_STATUS_2 register consists of one field: MPU_STIM_INTRQ_ST.

MPU_STIM_INTRQ_ST, IO, Address 0x48[7] (Read Only)

MPU_STIM_INTRQ_ST is the latched signal status of manual forced interrupt signal. Once set, this bit remains high until the interrupt is cleared via MPU_STIM_INTRQ_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 363. MPU_STIM_INTRQ_ST Function Description

MPU_STIM_INTRQ_ST	Description
0 (default)	Forced manual interrupt event has not occurred.
1	Force manual interrupt even has occurred.

The INTERRUPT_STATUS_6 register consists of the following fields: CP_LOCK_CH1_ST, CP_UNLOCK_CH1_ST, and STDI_DVALID_CH1_ST.

CP_LOCK_CH1_ST, IO, Address 0x5C[3] (Read Only)

Table 364. CP_LOCK_CH1_ST Function Description

CP_LOCK_CH1_ST	Description
0 (default)	No change. An interrupt has not been generated from this register.
1	Channel 1 CP input has caused the decoder to go from an unlocked state to a locked state.

CP_UNLOCK_CH1_ST, IO, Address 0x5C[2] (Read Only)

Table 365. CP_UNLOCK_CH1_ST Function Description

CP_UNLOCK_CH1_ST	Description
0 (default)	No change. An interrupt has not been generated from this register.
1	Channel 1 CP input has changed from a locked state to an unlocked state and has triggered an interrupt.

STDI_DVALID_CH1_ST, IO, Address 0x5C[1] (Read Only)

Latched signal status of STDI valid for Sync Channel 1 interrupt signal. Once set, this bit remains high until the interrupt is cleared via STDI_DATA_VALID_CH1_CLR. This bit is only valid if enabled via the corresponding INT1interrupt mask bit.

Table 366. STDI_DVALID_CH1_ST Function Description

STDI_DVALID_CH1_ST	Description
0 (default)	No STDI valid for sync Channel 1 interrupt has occurred.
1	A STDI valid for sync Channel 1 interrupt has occurred.

The HDMI Level Interrupt Status 1 register consists of the following fields: ISRC2_PCKT_ST, ISRC1_PCKT_ST, ACP_PCKT_ST, VS_INFO_ST, MS_INFO_ST, SPD_INFO_ST, and AUDIO_INFO_ST.

ISRC2_PCKT_ST, IO, Address 0x61[7] (Read Only)

ISRC2_PCKT_ST is the latched status of ISRC2 packet detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via ISRC2_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 367. ISRC2_PCKT_ST Function Description

ISRC2_PCKT_ST	Description
0 (default)	No interrupt generated from this register.
1	ISRC2_PCKT_RAW has changed. Interrupt has been generated.

ISRC1_PCKT_ST, IO, Address 0x61[6] (Read Only)

ISRC1_PCKT_ST is the latched status of ISRC1 packet detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via ISRC1_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 368. ISRC1_PCKT_ST Function Description

ISRC1_PCKT_ST	Description
0 (default)	No interrupt generated from this register.
1	ISRC1_PCKT_RAW has changed. Interrupt has been generated.

ACP_PCKT_ST, IO, Address 0x61[5] (Read Only)

ACP_PCKT_ST is the latched status of audio content protection packet detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via ACP_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 369. ACP_PCKT_ST Function Description

ACP_PCKT_ST	Description
0 (default)	No interrupt generated from this register.
1	ACP_PCKT_RAW has changed. Interrupt has been generated.

VS_INFO_ST, IO, Address 0x61[4] (Read Only)

VS_INFO_ST is the latched status of vendor specific InfoFrame detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via VS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 370. VS_INFO_ST Function Description

VS_INFO_ST	Description
0 (default)	No interrupt generated from this register.
1	VS_INFO_RAW has changed. Interrupt has been generated.

MS_INFO_ST, IO, Address 0x61[3] (Read Only)

MS_INFO_ST is the latched status of MPEG source InfoFrame detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via MS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 371. MS_INFO_ST Function Description

MS_INFO_ST	Description
0 (default)	No interrupt generated from this register.
1	MS_INFO_RAW has changed. Interrupt has been generated.

SPD_INFO_ST, IO, Address 0x61[2] (Read Only)

SPD_INFO_ST is the latched status of SPD InfoFrame detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via SPD_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 372. SPD_INFO_ST Function Description

SPD_INFO_ST	Description
0 (default)	No interrupt generated from this register.
1	SPD_INFO_RAW has changed. Interrupt has been generated.

AUDIO_INFO_ST, IO, Address 0x61[1] (Read Only)

AUDIO_INFO_ST is the latched status of audio InfoFrame detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via AUDIO_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 373. AUDIO_INFO_ST Function Description

AUDIO_INFO_ST	Description
0 (default)	No interrupt generated from this register.
1	AUDIO_INFO_RAW has changed. Interrupt has been generated.

AVI_INFO_ST, IO, Address 0x61[0] (Read Only)

For a detailed description, see the entry in the Interrupt Architecture Overview section.

HDMI Level Interrupt Status 2 is an 8-bit register, 0x66[7:0].

The HDMI Level Interrupt Status 2 register consists of the following fields: CS_DATA_VALID_ST, INTERNAL_MUTE_ST, AV_MUTE_ST, AUDIO_CH_MD_ST, HDMI_MODE_ST, GEN_CTL_PCKT_ST, AUDIO_C_PCKT_ST, and GAMUT_MDATA_ST.

CS_DATA_VALID_ST, IO, Address 0x66[7] (Read Only)

CS_DATA_VALID_ST is the latched status of channel status data valid interrupt signal. Once set, this bit remains high until the interrupt is cleared via ICS_DATA_VALID_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 374. CS_DATA_VALID_ST Function Description

CS_DATA_VALID_ST	Description
0 (default)	CS_DATA_VALID_RAW has not changed. An interrupt has not been generated.
1	CS_DATA_VALID_RAW has changed. An interrupt has been generated.

INTERNAL_MUTE_ST, IO, Address 0x66[6] (Read Only)

INTERNAL_MUTE_ST is the latched status of internal mute interrupt signal. Once set, this bit remains high until the interrupt is cleared via INTERNAL_MUTE_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 375. INTERNAL_MUTE_ST Function Description

INTERNAL_MUTE_ST	Description
0 (default)	INTERNAL_MUTE_RAW has not changed. An interrupt has not been generated.
1	INTERNAL_MUTE_RAW has changed. An interrupt has been generated.

AV_MUTE_ST, IO, Address 0x66[5] (Read Only)

AV_MUTE_ST is the latched status of AV mute detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via AV_MUTE_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 376. AV_MUTE_ST Function Description

AV_MUTE_ST	Description
0 (default)	AV_MUTE_RAW has not changed. An interrupt has not been generated.
1	AV_MUTE_RAW has changed. An interrupt has been generated.

AUDIO_CH_MD_ST, IO, Address 0x66[4] (Read Only)

AUDIO_CH_MD_ST is the latched status of audio channel mode interrupt signal. Once set, this bit remains high until the interrupt is cleared via AUDIO_CH_MD_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 377. AUDIO_CH_MD_ST Function Description

AUDIO_CH_MD_ST	Description
0 (default)	AUDIO_CH_MD_RAW has not changed. An interrupt has not been generated.
1	AUDIO_MODE_CHNG_RAW has changed. An interrupt has been generated.

HDMI_MODE_ST, IO, Address 0x66[3] (Read Only)

HDMI_MODE_ST is the latched status of HDMI mode interrupt signal. Once set, this bit remains high until the interrupt is cleared via HDMI_MODE_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 378. HDMI_MODE_ST Function Description

HDMI_MODE_ST	Description
0 (default)	HDMI_MODE_RAW has not changed. An interrupt has not been generated.
1	HDMI_MODE_RAW has changed. An interrupt has been generated.

GEN_CTL_PCKT_ST, IO, Address 0x66[2] (Read Only)

GEN_CTL_PCKT_ST is the latched status of general control packet interrupt signal. Once set, this bit remains high until the interrupt is cleared via GEN_CTL_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 379. GEN_CTL_PCKT_ST Function Description

GEN_CTL_PCKT_ST	Description
0 (default)	GEN_CTL_PCKT_RAW has not changed. Interrupt has not been generated from this register.
1	GEN_CTL_PCKT_RAW has changed. Interrupt has been generated from this register.

AUDIO_C_PCKT_ST, IO, Address 0x66[1] (Read Only)

AUDIO_C_PCKT_ST is the latched status of audio clock regeneration packet interrupt signal. Once set, this bit remains high until the interrupt is cleared via AUDIO_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 380. AUDIO_C_PCKT_ST Function Description

AUDIO_C_PCKT_ST	Description
0 (default)	AUDIO_C_PCKT_RAW has not changed. Interrupt has not been generated from this register.
1	AUDIO_C_PCKT_RAW has changed. Interrupt has been generated from this register.

GAMUT_MDATA_ST, IO, Address 0x66[0] (Read Only)

GAMUT_MDATA_ST is the latched status of gamut metadata packet detected interrupt signal. Once set, this bit remains high until the interrupt is cleared via GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 381. GAMUT_MDATA_ST Function Description

GAMUT_MDATA_ST	Description
0 (default)	GAMUT_MDATA_RAW has not changed. Interrupt has not been generated from this register.
1	GAMUT_MDATA_RAW has changed. Interrupt has been generated from this register.

The HDMI Level Interrupt Status 3 register consists of the following fields: CABLE_DET_B_ST, TMDSPLL_LCK_A_ST, TMDS_CLK_A_ST, VIDEO_3D_ST, V_LOCKED_ST, and DE_REGEN_LCK_ST.

TMDSPLL_LCK_A_ST, IO, Address 0x6B[6] (Read Only)

TMDSPLL_LCK_A_ST is the latched status of Port A TMDS PLL lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via TMDSPLL_LCK_A_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 382. TMDSPLL_LCK_A_ST Function Description

TMDSPLL_LCK_A_ST	Description
0 (default)	TMDSPLL_LCK_A_RAW has not changed. An interrupt has not been generated.
1	TMDSPLL_LCK_A_RAW has changed. An interrupt has been generated.

TMDS_CLK_A_ST, IO, Address 0x6B[4] (Read Only)

TMDS_CLK_A_ST is the latched status of Port A TMDS clock detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via TMDS_CLK_A_CLR. This bit is only valid if enabled via the corresponding INT1interrupt mask bit.

Table 383. TMDS_CLK_A_ST Function Description

TMDS_CLK_A_ST	Description
0 (default)	TMDS_CLK_A_RAW has not changed. An interrupt has not been generated.
1	TMDS_CLK_A_RAW has changed. An interrupt has been generated.

VIDEO_3D_ST, IO, Address 0x6B[2] (Read Only)

VIDEO_3D_ST is the latched status for the video 3D interrupt. Once set, this bit remains high until the interrupt is cleared via VIDEO_3D_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 384. VIDEO_3D_ST Function Description

VIDEO_3D_ST	Description
0 (default)	VIDEO_3D_RAW has not changed. An interrupt has not been generated.
1	VIDEO_3D_RAW has changed. An interrupt has been generated.

V_LOCKED_ST, IO, Address 0x6B[1] (Read Only)

V_LOCKED_ST is the latched status for the vertical sync filter locked interrupt. Once set, this bit remains high until the interrupt is cleared via V_LOCKED_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 385. V_LOCKED_ST Function Description

V_LOCKED_ST	Description
0 (default)	V_LOCKED_RAW has not changed. An interrupt has not been generated.
1	V_LOCKED_RAW has changed. An interrupt has been generated.

DE_REGEN_LCK_ST, IO, Address 0x6B[0] (Read Only)

DE_REGEN_LCK_ST is the latched status for DE regeneration lock interrupt signal. Once set, this bit remains high until the interrupt is cleared via DE_REGEN_LCK_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 386. DE_REGEN_LCK_ST Function Description

DE_REGEN_LCK_ST	Description
0 (default)	DE_REGEN_LCK_RAW has not changed. An interrupt has not been generated.
1	DE_REGEN_LCK_RAW has changed. An interrupt has been generated.

The HDMI Level Interrupt Status 4 register consists of the following fields: HDMI_ENCRPT_A_ST and CABLE_DET_A_ST.

HDMI_ENCRPT_A_ST, IO, Address 0x70[2] (Read Only)

HDMI_ENCRPT_A_ST is the latched status for Port A encryption detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via HDMI_ENCRPT_A_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 387. HDMI_ENCRPT_A_ST Function Description

HDMI_ENCRPT_A_ST	Description
0 (default)	HDMI_ENCRPT_A_RAW has not changed. An interrupt has not been generated.
1	HDMI_ENCRPT_A_RAW has changed. An interrupt has been generated.

CABLE_DET_A_ST, IO, Address 0x70[0] (Read Only)

CABLE_DET_A_ST is the latched status for Port A +5 V cable detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via CABLE_DET_A_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 388. CABLE_DET_A_ST Function Description

CABLE_DET_A_ST	Description
0 (default)	CABLE_DET_A_RAW has not changed. Interrupt has not been generated from this register.
1	CABLE_DET_A_RAW has changed. Interrupt has been generated from this register.

The HDMI Edge Interrupt Status 1 register consists of the following fields: NEW_ISRC2_PCKT_ST, NEW_ISRC1_PCKT_ST, NEW_ACP_PCKT_ST, NEW_VS_INFO_ST, NEW_MS_INFO_ST, NEW_SPD_INFO_ST, and NEW_AUDIO_INFO_ST.

NEW_ISRC2_PCKT_ST, IO, Address 0x7A[7] (Read Only)

NEW_ISRC2_PCKT_ST is the latched status for the new ISRC2 packet interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_ISRC2_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 389. NEW_ISRC2_PCKT_ST Function Description

NEW_ISRC2_PCKT_ST	Description
0 (default)	No new ISRC2 packet received. An interrupt has not been generated.
1	ISRC2 packet with new content received. An interrupt has been generated.

NEW_ISRC1_PCKT_ST, IO, Address 0x7A[6] (Read Only)

NEW_ISRC1_PCKT_ST is the latched status for the new ISRC1 packet interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_ISRC1_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 390. NEW_ISRC1_PCKT_ST Function Description

NEW_ISRC1_PCKT_ST	Description
0 (default)	No new ISRC1 packet received. An interrupt has not been generated.
1	ISRC1 packet with new content received. An interrupt has been generated.

NEW_ACP_PCKT_ST, IO, Address 0x7A[5] (Read Only)

NEW_ACP_PCKT_ST is the latched status for the new ACP packet interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_ACP_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 391. NEW_ACP_PCKT_ST Function Description

NEW_ACP_PCKT_ST	Description
0 (default)	No new ACP packet received. An interrupt has not been generated.
1	ACP packet with new content received. An interrupt has been generated.

NEW_VS_INFO_ST, IO, Address 0x7A[4] (Read Only)

NEW_VS_INFO_ST is the latched status for the new vendor specific InfoFrame interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_VS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 392. NEW_VS_INFO_ST Function Description

NEW_VS_INFO_ST	Description
0 (default)	No new VS packet received. An interrupt has not been generated.
1	VS packet with new content received. An interrupt has been generated.

NEW_MS_INFO_ST, IO, Address 0x7A[3] (Read Only)

NEW_MS_INFO_ST is the latched status for the new MPEG source InfoFrame interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_MS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 393. NEW_MS_INFO_ST Function Description

NEW_MS_INFO_ST	Description
0 (default)	No new MPEG Source InfoFrame received. Interrupt has not been generated.
1	MPEG Source InfoFrame with new content received. Interrupt has been generated.

NEW_SPD_INFO_ST, IO, Address 0x7A[2] (Read Only)

NEW_SPD_INFO_ST is the latched status for the new source product descriptor InfoFrame interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_SPD_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 394. NEW_SPD_INFO_ST Function Description

NEW_SPD_INFO_ST	Description
0 (default)	No new SPD InfoFrame received. Interrupt has not been generated.
1	SPD InfoFrame with new content received. Interrupt has been generated.

NEW_AUDIO_INFO_ST, IO, Address 0x7A[1] (Read Only)

NEW_AUDIO_INFO_ST is the latched status for the new audio InfoFrame interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_AUDIO_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 395. NEW_AUDIO_INFO_ST Function Description

NEW_AUDIO_INFO_ST	Description
0 (default)	No new Audio InfoFrame received. Interrupt has not been generated.
1	Audio InfoFrame with new content received. Interrupt has been generated.

NEW_AVI_INFO_ST, IO, Address 0x7A[0] (Read Only)

A detailed description of this function is available in the Interrupt Architecture Overview section.

The HDMI Edge Interrupt Status 2 register consists of the following fields: FIFO_NEAR_OVFL_ST, FIFO_UNDERFLO_ST, FIFO_OVERFLO_ST, CTS_PASS_THRSH_ST, CHANGE_N_ST, PACKET_ERROR_ST, AUDIO_PCKT_ERR_ST, and NEW_GAMUT_MDATA_ST.

FIFO_NEAR_OVFL_ST, IO, Address 0x7F[7] (Read Only)

This bit is the latched status for the audio FIFO near overflow interrupt. Once set, this bit remains high until the interrupt is cleared via FIFO_OVFL_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 396. FIFO_NEAR_OVFL_ST Function Description

FIFO_NEAR_OVFL_ST	Description
0 (default)	Audio FIFO has not reached high threshold.
1	Audio FIFO has reached high threshold.

FIFO_UNDERFLO_ST, IO, Address 0x7F[6] (Read Only)

This bit is the latched status for the audio FIFO underflow interrupt. Once set, this bit remains high until the interrupt is cleared via FIFO_UNDERFLO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 397. FIFO_UNDERFLO_ST Function Description

FIFO_UNDERFLO_ST	Description
0 (default)	Audio FIFO has not underflowed.
1	Audio FIFO has underflowed.

FIFO_OVERFLO_ST, IO, Address 0x7F[5] (Read Only)

This bit is the latched status for the audio FIFO overflow interrupt. Once set, this bit remains high until the interrupt is cleared via FIFO_OVERFLO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 398. FIFO_OVERFLO_ST Function Description

FIFO_OVERFLO_ST	Description
0 (default)	Audio FIFO has not overflowed.
1	Audio FIFO has overflowed.

CTS_PASS_THRSH_ST, IO, Address 0x7F[4] (Read Only)

This bit is the latched status for the ACR CTS value exceed threshold interrupt. Once set, this bit remains high until the interrupt is cleared via CTS_PASS_THRSH_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 399. CTS_PASS_THRSH_ST Function Description

CTS_PASS_THRSH_ST	Description
0 (default)	Audio clock regeneration CTS value has not passed the threshold.
1	Audio clock regeneration CTS value has changed more than threshold.

CHANGE_N_ST, IO, Address 0x7F[3] (Read Only)

This bit is the latched status for the ACR N value changed interrupt. Once set, this bit remains high until the interrupt is cleared via CHANGE_N_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 400. CHANGE_N_ST Function Description

CHANGE_N_ST	Description
0 (default)	Audio clock regeneration N value has not changed.
1	Audio clock regeneration N value has changed.

PACKET_ERROR_ST, IO, Address 0x7F[2] (Read Only)

This bit is the latched status for the packet error interrupt. Once set, this bit remains high until the interrupt is cleared via PACKET_ERROR_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 401. PACKET_ERROR_ST Function Description

PACKET_ERROR_ST	Description
0 (default)	No uncorrectable error detected in packet header. An interrupt has not been generated.
1	Uncorrectable error detected in an unknown packet (in packet header). An interrupt has been generated.

AUDIO_PCKT_ERR_ST, IO, Address 0x7F[1] (Read Only)

This bit is the latched status for the audio packet error interrupt. Once set, this bit remains high until the interrupt is cleared via AUDIO_PCKT_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 402. AUDIO_PCKT_ERR_ST Function Description

AUDIO_PCKT_ERR_ST	Description
0 (default)	No uncorrectable error detected in audio packets. An interrupt has not been generated.
1	Uncorrectable error detected in an audio packet. An interrupt has been generated.

NEW_GAMUT_MDATA_ST, IO, Address 0x7F[0] (Read Only)

This bit is the latched status for the new gamut metadata packet interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 403. NEW_GAMUT_MDATA_ST Function Description

NEW_GAMUT_MDATA_ST	Description
0 (default)	No new Gamut metadata packet received or no change has taken place. An interrupt has not been generated.
1	New Gamut metadata packet received. An interrupt has been generated.

The HDMI Edge Interrupt Status 3 register consists of the following fields: DEEP_COLOR_CHNG_ST, VCLK_CHNG_ST, AUDIO_MODE_CHNG_ST, PARITY_ERROR_ST, NEW_SAMP_RT_ST, AUDIO_FLT_LINE_ST, NEW_TMDS_FRQ_ST, and FIFO_NEAR_UFLO_ST.

DEEP_COLOR_CHNG_ST, IO, Address 0x84[7] (Read Only)

This bit is the latched status of deep color mode change interrupt. Once set, this bit remains high until the interrupt is cleared via DEEP_COLOR_CHNG_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 404. DEEP_COLOR_CHNG_ST Function Description

DEEP_COLOR_CHNG_ST	Description
0 (default)	Deep color mode has not changed.
1	Change in deep color has been detected.

VCLK_CHNG_ST, IO, Address 0x84[6] (Read Only)

This bit is the latched status of video clock change interrupt. Once set, this bit remains high until the interrupt is cleared via VCLK_CHNG_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 405. VCLK_CHNG_ST Function Description

VCLK_CHNG_ST	Description
0 (default)	No irregular or missing pulse detected in TMDS clock
1	Irregular or missing pulses detected in TMDS clock

AUDIO_MODE_CHNG_ST, IO, Address 0x84[5] (Read Only)

This bit is the latched status of audio mode change interrupt. Once set, this bit remains high until the interrupt is cleared via AUDIO_MODE_CHNG_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 406. AUDIO_MODE_CHNG_ST Function Description

AUDIO_MODE_CHNG_ST	Description
0 (default)	Audio mode has not changed.
1	Audio mode has changed.

PARITY_ERROR_ST, IO, Address 0x84[4] (Read Only)

This bit is the latched status of parity error interrupt. Once set, this bit remains high until the interrupt is cleared via PARITY_ERROR_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 407. PARITY_ERROR_ST Function Description

PARITY_ERROR_ST	Description
0 (default)	No parity error detected in audio packets
1	Parity error detected in an audio packet

NEW_SAMP_RT_ST, IO, Address 0x84[3] (Read Only)

This bit is the latched status of new sampling rate interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_SAMP_RT_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 408. NEW_SAMP_RT_ST Function Description

NEW_SAMP_RT_ST	Description
0 (default)	Sampling rate bits of the channel status data on Audio Channel 0 have not changed.
1	Sampling rate bits of the channel status data on Audio Channel 0 have changed.

AUDIO_FLT_LINE_ST, IO, Address 0x84[2] (Read Only)

This bit is the latched status of new TMDS frequency interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_TMDS_FREQ_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 409. AUDIO_FLT_LINE_ST Function Description

AUDIO_FLT_LINE_ST	Description
0 (default)	Audio sample packet with flat line bit set has not been received.
1	Audio sample packet with flat line bit set has been received.

NEW_TMDS_FRQ_ST, IO, Address 0x84[1] (Read Only)

This bit is the latched status of new TMDS frequency interrupt. Once set, this bit remains high until the interrupt is cleared via NEW_TMDS_FREQ_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 410. NEW_TMDS_FRQ_ST Function Description

NEW_TMDS_FRQ_ST	Description
0 (default)	TMDS frequency has not changed by more than tolerance.
1	TMDS frequency has changed by more than tolerance.

FIFO_NEAR_UFLO_ST, IO, Address 0x84[0] (Read Only)

This bit is the latched status for the audio FIFO near underflow interrupt. Once set, this bit remains high until the interrupt is cleared via FIFO_UFLO_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 411. FIFO_NEAR_UFLO_ST Function Description

FIFO_NEAR_UFLO_ST	Description
0 (default)	Audio FIFO has not reached low threshold.
1	Audio FIFO has reached low threshold.

The HDMI Edge Status 4 register consists of the following fields: MS_INF_CKS_ERR_ST, SPD_INF_CKS_ERR_ST, AUD_INF_CKS_ERR_ST, AVI_INF_CKS_ERR_ST, RI_EXPIRED_A_ST, and AKSV_UPDATE_A_ST.

MS_INF_CKS_ERR_ST, IO, Address 0x89[7] (Read Only)

This bit is the latched status of MPEG source InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 412. MS_INF_CKS_ERR_ST Function Description

MS_INF_CKS_ERR_ST	Description
0 (default)	No change in MPEG source InfoFrame checksum error
1	An MPEG source InfoFrame checksum error has triggered this interrupt

SPD_INF_CKS_ERR_ST, IO, Address 0x89[6] (Read Only)

This bit is the latched status of SPD InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via SPD_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 413. SPD_INF_CKS_ERR_ST Function Description

SPD_INF_CKS_ERR_ST	Description
0 (default)	No change in SPD InfoFrame checksum error
1	An SPD InfoFrame checksum error has triggered this interrupt

AUD_INF_CKS_ERR_ST, IO, Address 0x89[5] (Read Only)

This bit is the latched status of audio InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via AUDIO_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 414. AUD_INF_CKS_ERR_ST Function Description

AUD_INF_CKS_ERR_ST	Description
0 (default)	No change in audio InfoFrame checksum error
1	An audio InfoFrame checksum error has triggered this interrupt

AVI_INF_CKS_ERR_ST, IO, Address 0x89[4] (Read Only)

This bit is the latched status of AVI InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via AVI_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 415. AVI_INF_CKS_ERR_ST Function Description

AVI_INF_CKS_ERR_ST	Description
0 (default)	No change in AVI InfoFrame checksum error
1	An AVI InfoFrame checksum error has triggered this interrupt

RI_EXPIRED_A_ST, IO, Address 0x89[2] (Read Only)

This bit is the latched status of Port A Ri expired interrupt. Once set, this bit remains high until the interrupt is cleared via RI_EXPIRED_A_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 416. RI_EXPIRED_A_ST Function Description

RI_EXPIRED_A_ST	Description
0 (default)	No Ri expired on Port A
1	Ri expired on Port A

AKSV_UPDATE_A_ST, IO, Address 0x89[0] (Read Only)

This bit is the latched status of Port A AKSV update interrupt. Once set, this bit remains high until the interrupt is cleared via AKSV_UPDATE_A_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 417. AKSV_UPDATE_A_ST Function Description

AKSV_UPDATE_A_ST	Description
0 (default)	No AKSV updates on Port A
1	Detected a write access to the AKSV register on Port A

HDMI Edge Interrupt Status 5 register consists of the VS_INF_CKS_ERR_ST field.

BG_MEAS_DONE_ST, IO, Address 0x8E[1] (Read Only)

This bit is the latched status of background port measurement completed interrupt. Once set, this bit remains high until the interrupt has been cleared via BG_MEAS_DONE_CLR. This bit is only valid if enabled via corresponding the INT1 interrupt mask bit.

Table 418. BG_MEAS_DONE_ST Function Description

BG_MEAS_DONE_ST	Description
0 (default)	Measurements of TMDS frequency and video parameters of background port not finished or not requested.
1	Measurements of TMDS frequency and video parameters of background port are ready

VS_INF_CKS_ERR_ST, IO, Address 0x8E[0] (Read Only)

This bit is the latched status of MPEG source InfoFrame checksum error interrupt. Once set, this bit remains high until the interrupt is cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 interrupt mask bit.

Table 419. VS_INF_CKS_ERR_ST Function Description

VS_INF_CKS_ERR_ST	Description
0 (default)	No change in VS InfoFrame checksum error
1	A VS InfoFrame checksum error has triggered this interrupt

The CEC_STATUS1_INT_STATUS register consists of the following fields:

- CEC_RX_RDY2_ST
- CEC_RX_RDY1_ST
- CEC_RX_RDY0_ST
- CEC_TX_RETRY_TIMEOUT_ST
- CEC_TX_ARBITRATION_LOST_ST
- CEC_TX_READY_ST

The CEC_STATUS2_INT_STATUS register consists of the CEC_INTERRUPT_BYTE_ST[7:0] field.

CEC_INTERRUPT_BYTE_ST[7:0], IO, Address 0x98[7:0] (Read Only)

Table 420. CEC_INTERRUPT_BYTE_ST[7:0] Function Description

CEC_INTERRUPT_BYTE_ST[7:0]	Description
0 (default)	No change
1	One of the 8 opcodes received

REGISTER ACCESS AND SERIAL PORTS DESCRIPTION

The ADV7613 has three 2-wire serial (I²C-compatible) ports:

- One main I²C port, SDA/SCL, allows a system I²C master controller to control and configure the ADV7613.
- Two I²C ports, DDC Port A and Port B, allow an HDMI host to access the internal EDID and the HDCP registers.

MAIN I²C PORT

Register Access

The ADV7613 has eight 256-byte maps that can be accessed via the main I²C ports, SDA and SCL. Each map has its own I²C address and acts as a standard slave device on the I²C bus.

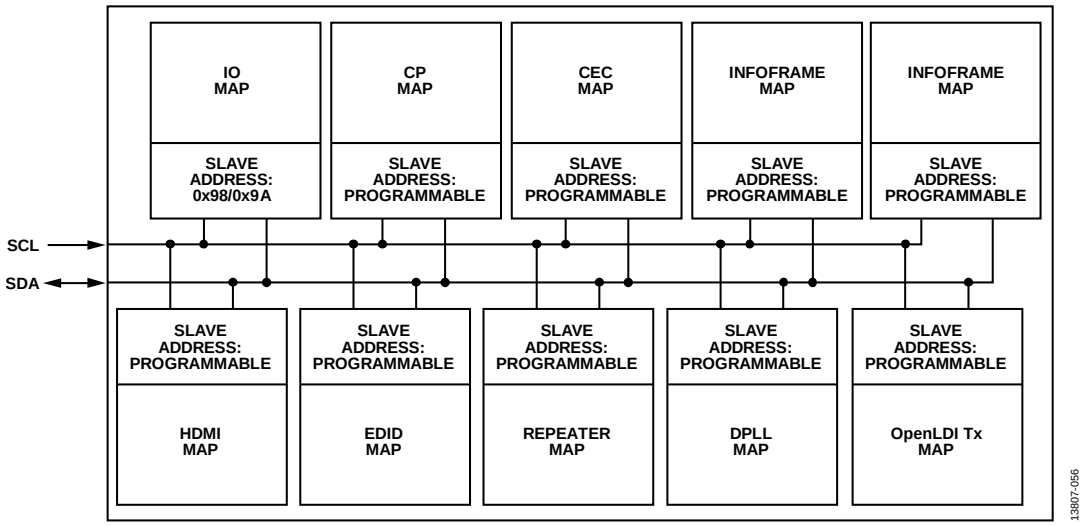

Figure 56. ADV7613 Register Map Access through Main I²C Port

Seven out of the eight maps have a programmable I²C address. This facilitates the integration of the ADV7613 in systems that have multiple slaves on the general I²C bus.

Table 421. Register Maps and I²C Addresses

Map	Default Address	Programmable Address	Location Where Address Can Be Programmed
IO Map	0x98	Not programmable	Not applicable
CP Map	0x00 (disabled)	Programmable	IO Map Register 0xFD
HDMI Map	0x00 (disabled)	Programmable	IO Map Register 0xFB
Repeater Map	0x00 (disabled)	Programmable	IO Map Register 0xF9
EDID Map	0x00 (disabled)	Programmable	IO Map Register 0xFA
InfoFrame Map	0x00 (disabled)	Programmable	IO Map Register 0xF5
CEC Map	0x00 (disabled)	Programmable	IO Map Register 0xF4
DPLL Map	0x00 (disabled)	Programmable	IO Map Register 0xF8
OpenLDI Tx Map	0x00 (disabled)	Programmable	IO Map Register 0xC0

Addresses of Other Maps

CEC_SLAVE_ADDR[6:0], IO, Address 0xF4[7:1]

CEC_SLAVE_ADDR[6:0] is the programmable I²C slave address for CEC map.

Table 422. CEC_SLAVE_ADDR[6:0] Function Description

CEC_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	CEC map slave address

INFOFRAME_SLAVE_ADDR[6:0], IO, Address 0xF5[7:1]

INFOFRAME_SLAVE_ADDR[6:0] is the programmable I²C slave address for InfoFrame map.

Table 423. INFOFRAME_SLAVE_ADDR[6:0] Function Description

INFOFRAME_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	InfoFrame map slave address

KSV_SLAVE_ADDR[6:0], IO, Address 0xF9[7:1]

KSV_SLAVE_ADDR[6:0] is the programmable I²C slave address for KSV (Repeater) map.

Table 424. KSV_SLAVE_ADDR[6:0] Function Description

KSV_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	Repeater map slave address

EDID_SLAVE_ADDR[6:0], IO, Address 0xFA[7:1]

EDID_SLAVE_ADDR[6:0] is the programmable I²C slave address for EDID map.

Table 425. EDID_SLAVE_ADDR[6:0] Function Description

EDID_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	EDID map slave address

HDMI_SLAVE_ADDR[6:0], IO, Address 0xFB[7:1]

HDMI_SLAVE_ADDR[6:0] is the programmable I²C slave address for HDMI map.

Table 426. HDMI_SLAVE_ADDR[6:0] Function Description

HDMI_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	HDMI map slave address

CP_SLAVE_ADDR[6:0], IO, Address 0xFD[7:1]

CP_SLAVE_ADDR[6:0] is the programmable I²C slave address for CP map.

Table 427. CP_SLAVE_ADDR[6:0] Function Description

CP_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	CP map slave address

DPLL_SLAVE_ADDR[6:0], IO, Address 0xF8[7:1]

DPLL_SLAVE_ADDR[6:0] is the programmable I²C slave address for DPLL map.

Table 428. DPLL_SLAVE_ADDR[6:0] Function Description

DPLL_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	DPLL map slave address

Protocol for Main I²C Port

The system controller initiates a data transfer by establishing a start condition, defined by a high to low transition on SDA while SCL remains high. This transition indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (7-bit address and R/W bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition.

In the idle condition, the device monitors the SDA and SCL lines for the start condition and the correct transmitted address. The R/W bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. A Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

Each of the ADV7613 maps acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/W bit. It interprets the first byte as the map address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, these cause an immediate jump to the idle condition. During a given SCLK high period, the user must issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7613 does not issue an acknowledge and returns to the idle condition.

If the user exceeds the highest subaddress in auto-increment mode, the following actions are taken:

- In read mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register. A no acknowledge is issued by the ADV7613, and the device returns to the idle condition.

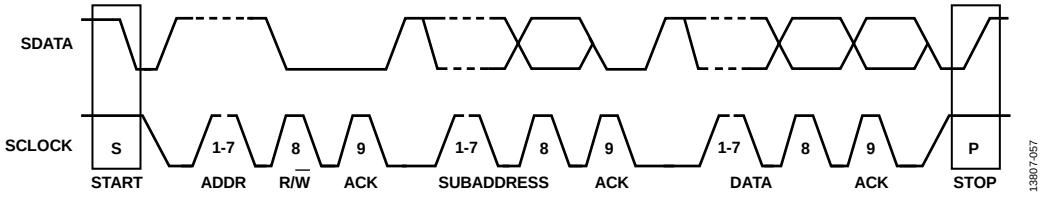

Figure 57. Bus Data Transfer

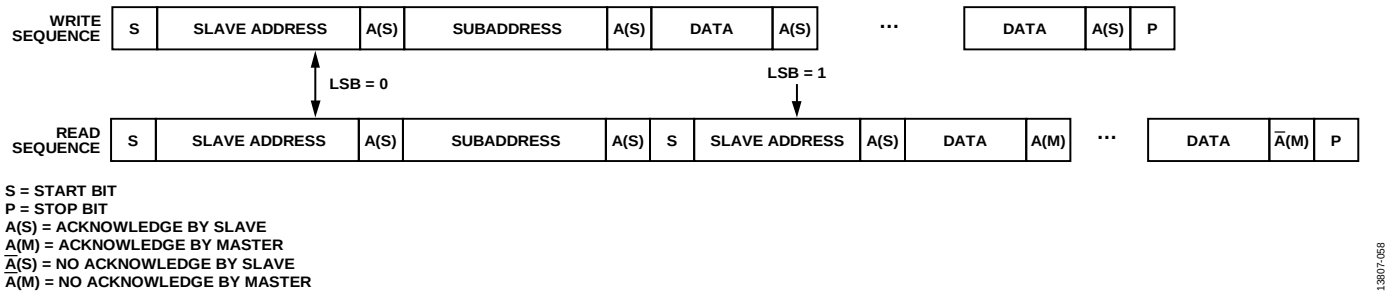

Figure 58. Read and Write Sequence

DDC PORTS

An I²C port, DDC Port A, allows HDMI hosts to access the internal E-EDID and the HDCP registers. Note that the DDC ports are 5 V tolerant, which simplifies the hardware between the HDMI connector and the ADV7613.

I²C Protocols for Access to the Internal EDID

An I²C master connected on a DDC port can access the internal EDID using the following protocol:

- Write sequence, as defined in the Protocol for Main I²C Port section.
- Read sequence, as defined in the Protocol for Main I²C Port section.
- Current address read sequence: allows the master on the DDC port to read access internal E-EDID without specifying the subaddress that must be read. The ADV7613 stores an address counter for DDC port that maintains the value of the subaddress that was last accessed. The address counter is incremented by one every time a read or a write access is requested on the DDC port.

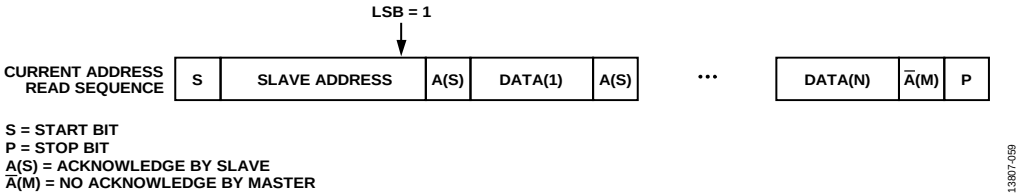

Figure 59. Current Address Read Sequence

I²C Protocols for Access to HDCP Registers

An I²C master connected on a DDC port can access the internal EDID using the following protocol:

- Write sequence, as defined in the Protocol for Main I²C Port section.
- Read sequence, as defined in the Protocol for Main I²C Port section.
- Short read format, as defined in the High-Bandwidth Digital Content Protection (HDCP) system specifications

DDC Port A

The DDC lines of the HDMI Port A comprise the DDCA_SCL and DDCA_SDA pins. An HDMI host connected to the DDC Port A accesses the internal E-EDID at address 0xA0 in read only mode, and the HDCP registers at address 0x74 in read/write mode (refer to Figure 60). The internal E-EDID for Port A is described in the Structure of Internal E-EDID for Port A section.

Refer to the HDCP system specifications for detailed information on the HDCP registers.

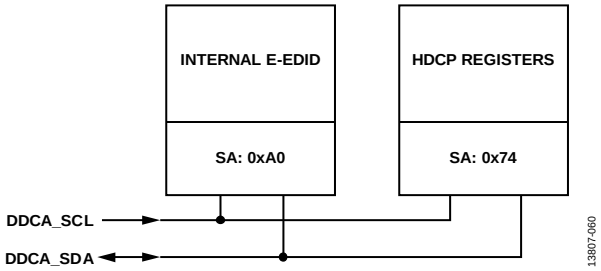

Figure 60. Internal E-EDID and HDCP Registers Access from Port A (SA = Slave Address)

LVDS TRANSMITTERS

INTRODUCTION

The ADV7613 features two LVDS transmitters that can be configured to output either 18 bits or 24 bits, and offers two mapping options.

The LVDS transmitters in dual mode connected to a dual LVDS panel outputs even pixel data on LVDS Transmitter 1 and odd pixel data on LVDS Transmitter 2.

In single LVDS transmitter mode, there is no splitting of the even and odd pixel data.

CONFIGURING THE LVDS TRANSMITTER

Follow these steps to configure the LVDS transmitter:

1. Power up the LVDS transmitter and enable its PLL.
2. Select the PLL gear.
3. Select the color depth (the default is eight bits per component).
4. Select mapping option (the default is OpenLDI bitmapping).
5. Set the polarity of the video timing control bits (the default is HS, VS, and DE active high).
6. In 8-bit color depth mode, set the value of the reserved (RES) bit if required (the default is 0).

ENABLING THE LVDS TRANSMITTER

To enable the LVDS transmitter, power up the transmitter and enable its PLL, using the following controls.

TX_PDN, OpenLDI Tx, Address 0x40[1]

TX_PDN powers down the LVDS transmitter.

Table 429. TX_PDN Function Description

TX_PDN	Description
0	Powered up
1	Powered down

TX_PLL_EN, OpenLDI Tx, Address 0x40[3]

TX_PLL_EN enables the PLL for the LVDS transmitter.

Table 430. TX_PLL_EN Function Description

TX_PLL_EN	Description
0	PLL disabled
1	PLL enabled

PLL GEAR SELECTION

The ADV7613 LVDS transmitter can output a maximum clock frequency of 92 MHz. The PLL gear must be set based on the output clock frequency. This is done by setting the following control.

TX_PLL_GEAR[2:0], OpenLDI Tx, Address 0x44[2:0]

TX_PLL_GEAR[2:0] sets the PLL gear to be used based on the LVDS output clock frequency.

Table 431. TX_PLL_GEAR[2:0] Function Description

TX_PLL_GEAR[2:0]	Description
000	0 to 200 MHz (default)
010	200 MHz to 300 MHz
xxx	Reserved

The ADV7613 can output graphics resolutions with clock frequency 25MHz to 92 MHz. For this range of graphics resolutions and frequencies mentioned, the PLL gear must be set as follows:

- From 25 MHz to 40 MHz: TX_PLL_GEAR[2:0] must be set to 000.
- From 40 MHz to 92 MHz: TX_PLL_GEAR[2:0] must be set to 010.

LVDS OUTPUT MODES

Color Depth Mode

The ADV7613 LVDS transmitter can output either 18-bit or 24-bit RGB data, that is, six bits or eight bits per color component. The color depth is set by the following control.

TX_COLOR_MODE, OpenLDI Tx, Address 0x4C[0]

TX_COLOR_MODE selects the color depth to be encoded in LVDS mode.

Table 432. TX_COLOR_MODE Function Description

TX_COLOR_MODE	Description
0	6 bits
1	8 bits

Note that there is no dithering block available for the LVDS transmitter output when outputting six bits per color component. If required, dithering must be done externally.

Bitmapping Mode

The ADV7613 LVDS transmitter offers two LVDS bitmapping options:

- OpenLDI mapping
- Alternative mapping

The bitmapping option can be selected using the following control.

TX_ENABLE_NS_MAPPING, OpenLDI Tx, Address 0x4C[3]

TX_ENABLE_NS_MAPPING enables alternative bitmapping in LVDS 8-bit modes.

Table 433. TX_ENABLE_NS_MAPPING Function Description

TX_ENABLE_NS_MAPPING	Description
0	OpenLDI bitmapping
1	Alternative bitmapping

OpenLDI mapping is available for both 6-bit and 8-bit output modes. Alternative mapping is available only in 8-bit output mode.

OpenLDI BITMAPPING WITH 6-BIT COLOR DEPTH

Figure 61 shows OpenLDI bitmapping with the 6-bit color depth that the ADV7613 can output. In this mode, the data is packed into three data lanes, carrying six bits for each color component along with the video timing controls—that is, active data enable (DE), vertical synchronization (VS), and horizontal synchronization (HS). The clock channel does not have a 50% duty cycle; instead, its falling edge is aligned to the start of the third component in the cycle, and its rising edge is aligned to the start of the sixth component in the cycle.

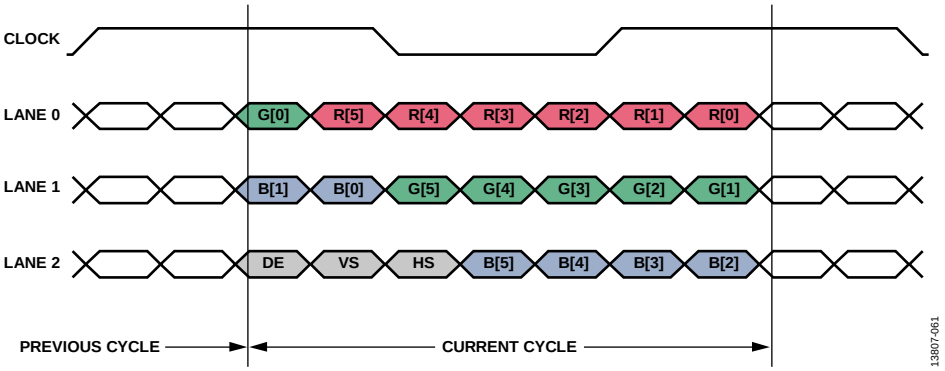

Figure 61. OpenLDI Mapping with 6-Bit Color Depth

OpenLDI BITMAPPING WITH 8-BIT COLOR DEPTH

Figure 62 shows OpenLDI bitmapping with the 8-bit color depth that the ADV7613 can output. This mode is a simple extension of the OpenLDI bitmapping with the 6-bit color depth described in the OpenLDI Bitmapping with 6-Bit Color Depth section, where each color component is extended to eight bits. The two LSBs for each color are placed on Lane 3, so that a receiver only capable of receiving 18-bit video still shows a reasonable picture. The bit labelled RES is reserved for future use.

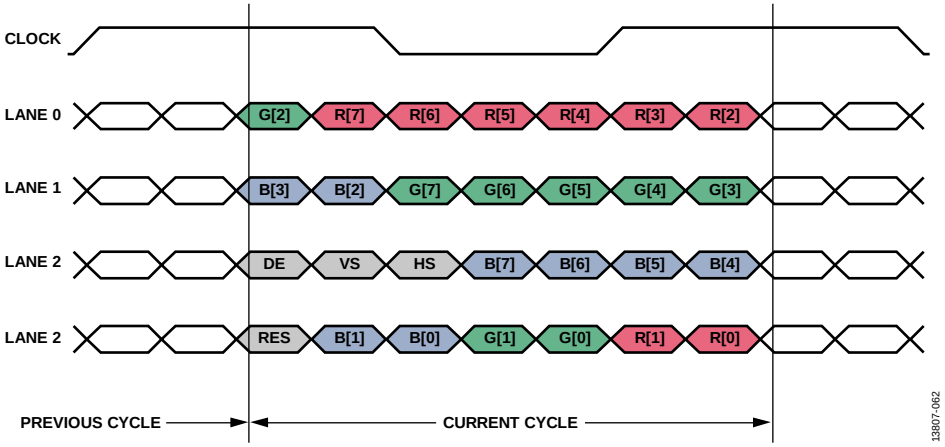

Figure 62. OpenLDI Mapping with 8-Bit Color Depth

ALTERNATIVE BITMAPPING (8-BIT COLOR DEPTH ONLY)

Figure 63 shows alternative bitmapping with the 8-bit color depth that the ADV7613 can output. In this mode, the data is packed into four data lanes carrying eight bits for each color component, along with the video timing controls—that is, active data enable (DE), vertical synchronization (VS), and horizontal synchronization (HS). The bit labelled RES is reserved for future use. Similar to OpenLDI bitmapping, the clock channel does not have a 50% duty cycle; instead, its falling edge is aligned to the start of the third component in the cycle, and its rising edge is aligned to the start of the sixth component in the cycle.

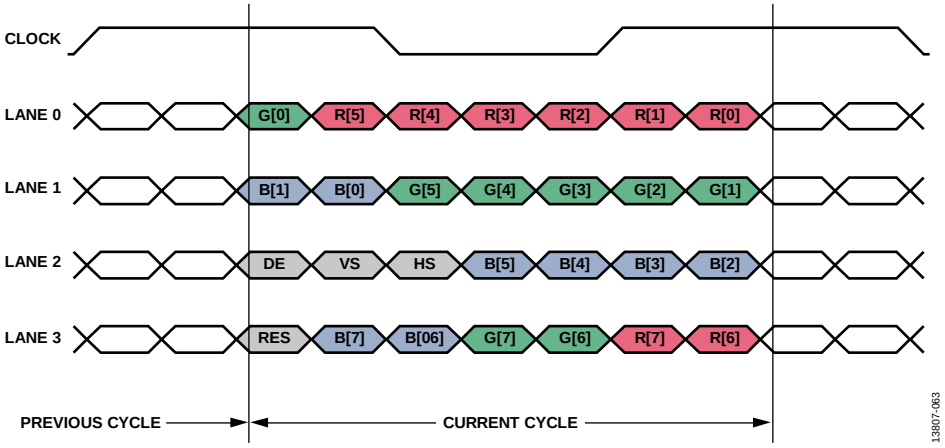

Figure 63. Alternative Bitmapping (8-Bit Color Depth Only)

POLARITY OF VIDEO TIMING CONTROL BITS

The polarity of the video timing control bits (HS, VS, and DE) can be defined using the following controls.

TX_OLDI_DE_POL, OpenLDI Tx, Address 0x4C[4]

TX_OLDI_DE_POL sets the DE polarity for output OpenLDI data.

Table 434. TX_OLDI_DE_POL Function Description

TX_OLDI_DE_POL	Description
0	DE is active low
1	DE is active high

TX_OLDI_VS_POL, OpenLDI Tx, Address 0x4C[5]

TX_OLDI_VS_POL sets the VS polarity for output OpenLDI data.

Table 435. TX_OLDI_VS_POL Function Description

TX_OLDI_VS_POL	Description
0	VSYNC is active low
1	VSYNC is active high

TX_OLDI_HS_POL, OpenLDI Tx, Address 0x4C[6]

TX_OLDI_HS_POL sets the HS polarity for output OpenLDI data.

Table 436. TX_OLDI_HS_POL Function Description

TX_OLDI_HS_POL	Description
0	HSYNC is active low
1	HSYNC is active high

RESERVED BIT CONTROL

Both OpenLDI bitmapping with 8-bit color depth and alternative bitmapping transmit a bit which is reserved for future use (labelled RES). By default, a fixed value of 0 is set for this bit. However, it is possible to set the value sent with the controls as described in this section.

TX_MUX_INT_RES, OpenLDI Tx, Address 0x4E[0]

TX_MUX_INT_RES enables programming of the reserved bit (RES) value in 8-bit color depth modes.

Table 437. TX_MUX_INT_RES Function Description

TX_MUX_INT_RES	Description
0	RES bit value is fixed to 0
1	RES bit value is defined by TX_INT_RES

TX_INT_RES, OpenLDI Tx, Address 0x4E[1]

When TX_MUX_INT_RES is set to 1, this control sets the value for the reserved bit (RES) in 8-bit color depth modes.

Table 438. TX_INT_RES Function Description

TX_INT_RES	Description
0	RES bit value is 0
1	RES bit value is 1

LVDS TRANSMITTER READBACK REGISTERS

The ADV7613 LVDS transmitter has a readback bit that indicates whether its PLL is locked or not.

TX_PLL_LOCK_DET, OpenLDI Tx, Address 0x4F[2] (Read Only)

TX_PLL_LOCK_DET is the readback of the LVDS PLL lock detect.

Table 439. TX_PLL_LOCK_DET Function Description

TX_PLL_LOCK_DET	Description
0	LVDS Tx PLL not locked
1	LVDS Tx PLL is locked

The ADV7613 LVDS transmitter also has readbacks that indicate whether the VS and HS, at their input s, have negative or positive polarity.

TX_DETECTED_HS_POL, OpenLDI Tx, Address 0x4F[0] (Read Only)

TX_DETECTED_HS_POL is the readback of the detected HS polarity used for LVDS Tx.

Table 440. TX_DETECTED_HS_POL Function Description

TX_DETECTED_HS_POL	Description
0	Incoming HSYNC to LVDS Tx is active low
1	HSYNC is active high

TX_DETECTED_VS_POL, OpenLDI Tx, Address 0x4F[1] (Read Only)

TX_DETECTED_VS_POL is the readback of the detected VS polarity used for LVDS Tx.

Table 441. TX_DETECTED_VS_POL Function Description

TX_DETECTED_VS_POL	Description
0	Incoming VSYNC to LVDS Tx is active low
1	VSYNC is active high

LVDS OUTPUT FORMATTER

The output formatter blocks splits a single video data stream into two separate streams, so that the even pixel stream is output on LVDS Transmitter 1, and the odd pixel stream is output on LVDS Transmitter 2, as shown in Figure 64.

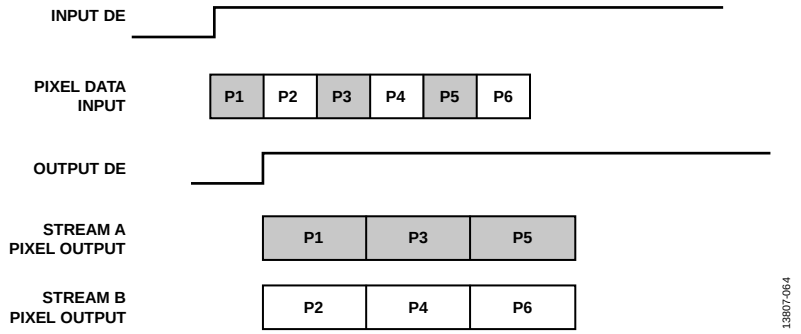

Figure 64. Odd and Even Pixel Streaming

TX_BYPASS_PIX_DEMUX, OpenLDI Tx, Address 0x4E[5]

This register disables the block that maps the output data into two separate LVDS output channels. When active, only one of the LVDS ports is active and sending data. The other port is disabled.

Table 442. TX_BYPASS_PIX_DEMUX Function Description

TX_BYPASS_PIX_DEMUX	Description
0	Enables 2 LVDS transmitters at same time to output data
1	Allows 1 LVDS transmitter output

TX_PIXEL_SWAP, OpenLDI Tx, Address 0x4E[4]

This register allows LVDS Output Port 1 to output even pixel data stream and LVDS Output Port 2 to output odd pixel data stream if set to zero (0). Do not set this bit to one (1) when enabling two LVDS transmitters mode (that is, when TX_BYPASS_PIX_DEMUX is 0).

Table 443. TX_PIXEL_SWAP Function Description

TX_PIXEL_SWAP	Description
0	Even pixel output data stream on Port 1 and odd pixel output data stream on Port 2 if TX_BYPASS_PIX_DEMUX is 0. Allows LVDS Port 2 output only if TX_BYPASS_PIX_DEMUX is 1.
1	Allows LVDS Port 1 output only if TX_BYPASS_PIX_DEMUX is 1

The combined effect of both I²C bits is summarized in Table 444.

Table 444. Pixel Swap and Demux

TX_BYPASS_PIX_DEMUX	TX_PIXEL_SWAP	LVDS Port 1 Output	LVDS Port 2 Output
0	0	P2/P4/P6/…	P1/P3/P5/…
1	0	0	P1/P2/P3/…
1	1	P1/P2/P3/…	0

PCB LAYOUT RECOMMENDATIONS

The ADV7613 is a high precision, high speed, mixed signal device. It is important to have a well laid out printed circuit board (PCB) to achieve the maximum performance from the device. The following sections are a guide for designing a board using the ADV7613.

POWER SUPPLY BYPASSING

It is recommended to bypass each power supply pin with a 0.1 µF and a 10 nF capacitor where possible. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin.

Physically locate the bypass capacitors between the power plane and the power pin. Current must flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Generally, the best approach is to place a via underneath the 100 nF capacitor pads down to the power plane (refer to Figure 65).

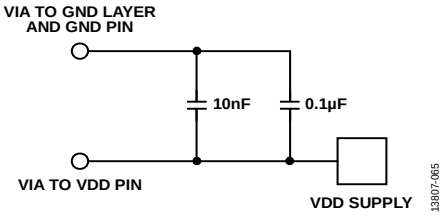

Figure 65. Recommended Power Supply Decoupling

It is particularly important to maintain low noise and good stability of the clock generator supply (PVDD). Abrupt changes in the PVDD supply can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated or heavily filtered supplies for each of the analog circuitry groups (CVDD, TVDD, and PVDD).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical synchronization periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PVDD, from a different, cleaner, power source, for example, from a 12 V supply.

It is also recommended to use a single ground plane for the entire board. Repeatedly, experience has shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to place, at least, a single ground plane under the ADV7613. It is important to place components wisely because the current loops are much longer when using split ground planes as the current takes the path of least resistance.

DIGITAL OUTPUTS (DATA AND CLOCKS)

The trace length that the digital outputs need to drive must be minimized. Longer traces have higher capacitance, which requires more current that can cause more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a series resistor of value between 33 Ω to 200 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside the ADV7613. If series resistors are used, they must be placed as close as possible to the ADV7613 pins, and the trace impedance for these signals must match that of the termination resistors selected.

If possible, the capacitance that each of the digital outputs drives must be limited to is less than 15 pF. This can be accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV7613, creating more digital noise on its power supplies.

DIGITAL INPUTS

The following digital inputs on the ADV7613 are 3.3 V inputs that are 5.0 V tolerant:

- DDCA_SCL
- DDCA_SDA

Any noise that gets onto the HS and VS inputs trace adds jitter to the system. Therefore, the trace length must be minimized; and digital or other high frequency traces must not be run near it.

XTAL AND LOAD CAP VALUE SELECTION

The ADV7613 uses a 28.6363 MHz crystal. Figure 66 shows an example of a reference clock circuit for the ADV7613. Special care must be taken when using a crystal circuit to generate the reference clock for the ADV7613. Small variations in reference clock frequency can cause automatic detection issues and impair the ADV7613 performance.

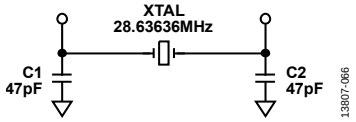

Figure 66. Crystal Circuit

Follow these guidelines to ensure correct operation:

- Use the correct frequency crystal, which is 28.6363 MHz. Tolerance must be 50 ppm or better.
- Know the C_{LOAD} for the crystal part number selected. The value of the C1 and C2 capacitors must be matched to the C_{LOAD} for the specific crystal part number in the system of the user.

To find C1 and C2, use the following formula:

$$C1 = C2 = 2(C_{LOAD} - C_{STRAY}) - C_{PG}$$

where:
C_{STRAY} is usually 2 pF to 3 pF, depending on the board traces.
C_{PG} (pin to ground capacitance) is 4 pF for the ADV7613.

For example, C_{LOAD} = 30 pF, C1 = 50 pF, and C2 = 50 pF. In this case, 47 pF is the nearest real-life capacitor value to 50 pF.